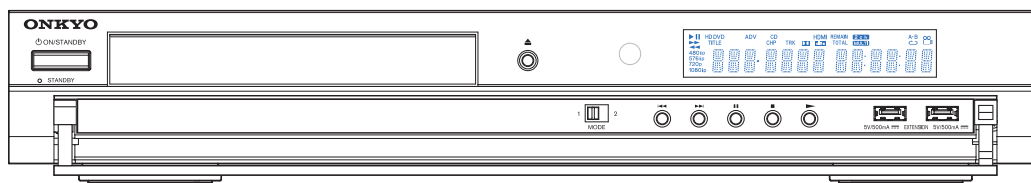


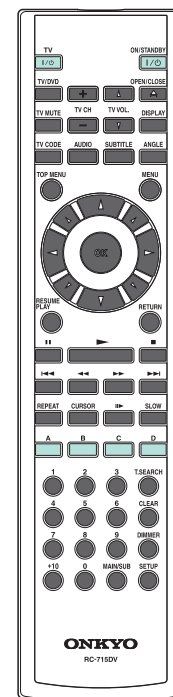
ONKYO SERVICE MANUAL

HD DVD PLAYER MODEL DX-HD805




Black models

BCDD	120V AC, 60Hz
BCMP	220-240V AC, 50/60Hz



RC-715DV

SAFETY-RELATED COMPONENT WARNING!!

COMPONENTS IDENTIFIED BY MARK  ON THE SCHEMATIC DIAGRAM AND IN THE PARTS LIST ARE CRITICAL FOR RISK OF FIRE AND ELECTRIC SHOCK. REPLACE THESE COMPONENTS WITH ONKYO PARTS WHOSE PART NUMBERS APPEAR AS SHOWN IN THIS MANUAL.

MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

BLOCK DIAGRAM

1

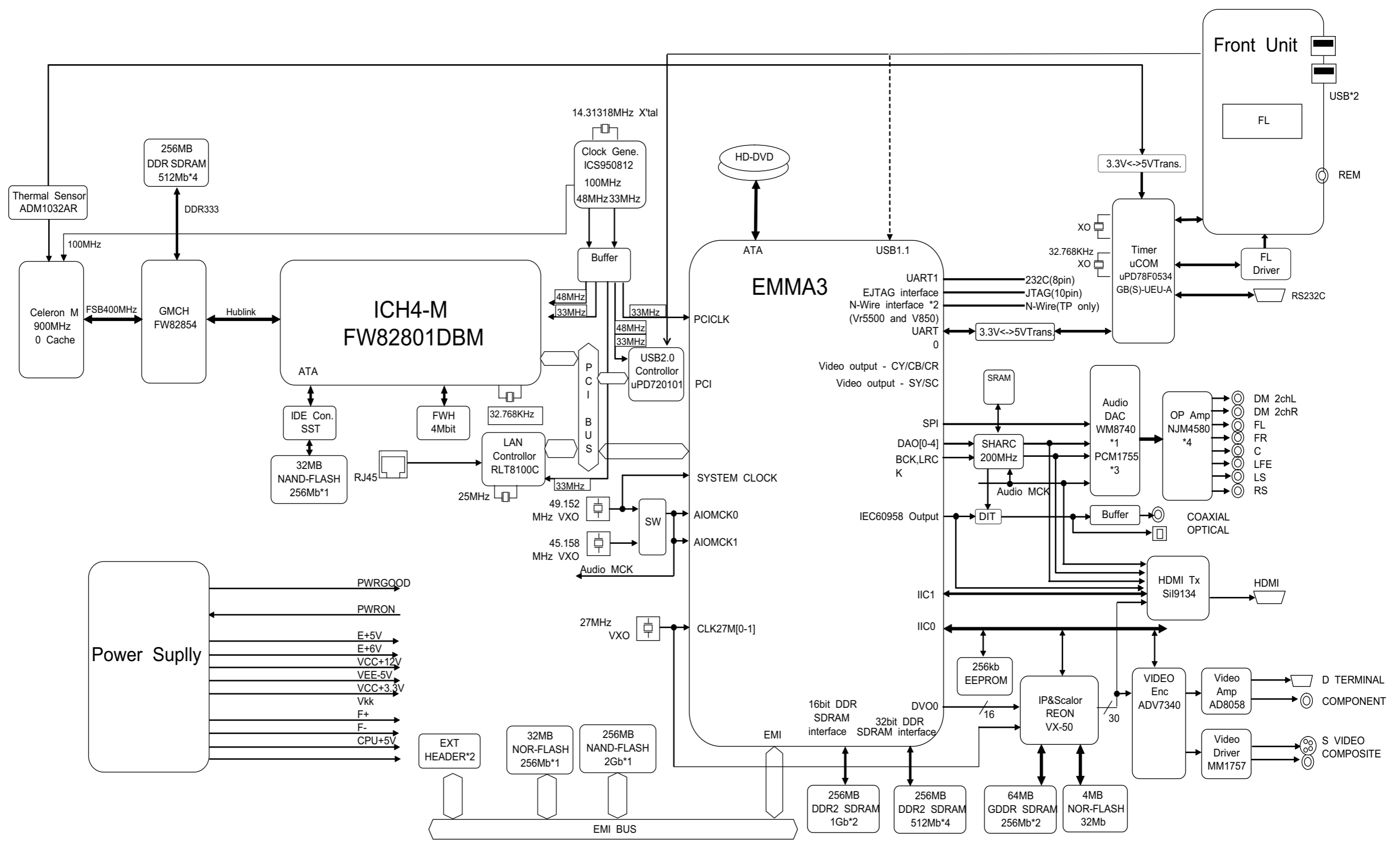
2

3

4

5

A B C D E F G H



WIRERING CONNECTION DIAGRAM

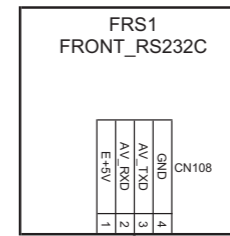
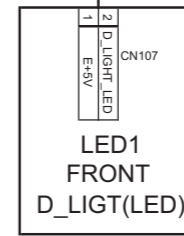
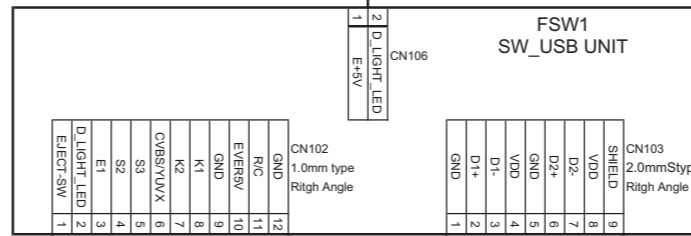
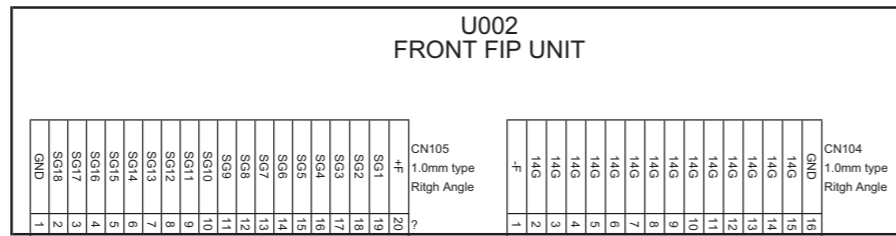
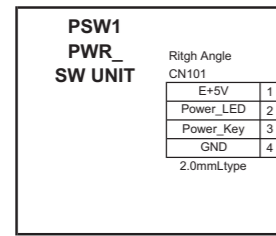
1

2

3

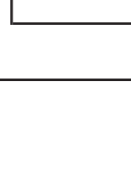
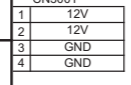
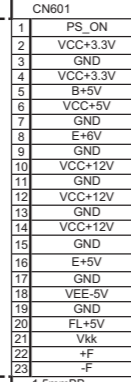
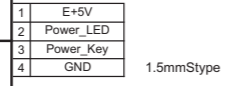
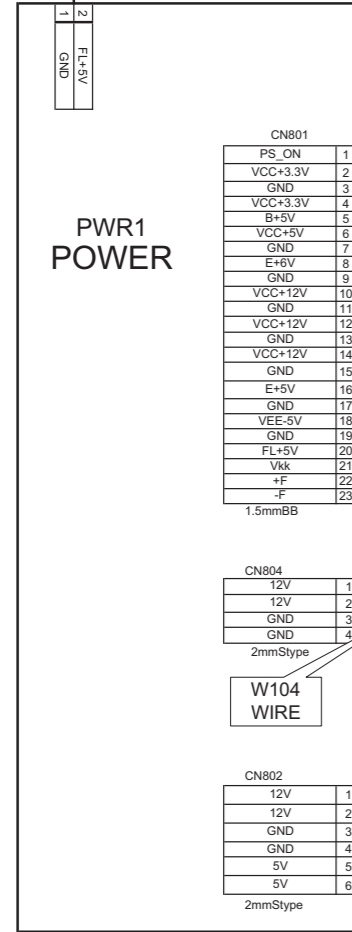
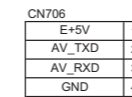
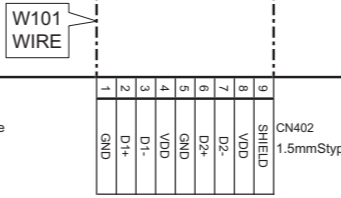
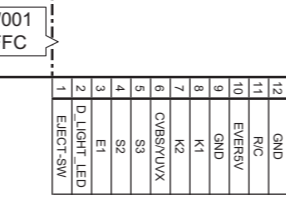
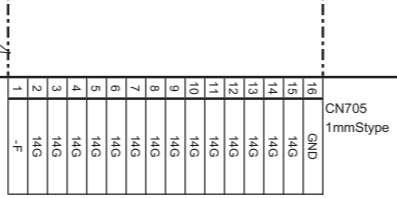
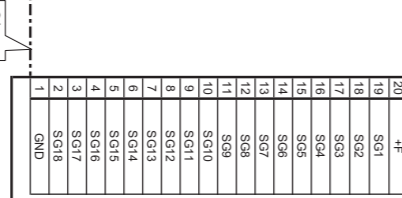
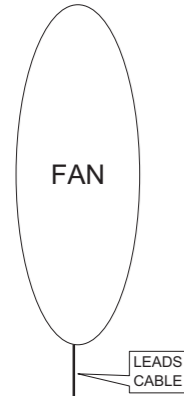
4

5

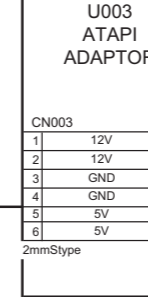
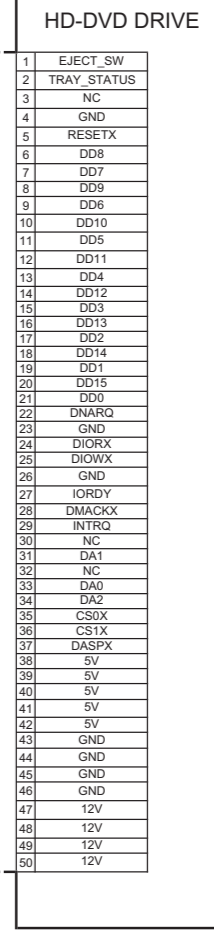
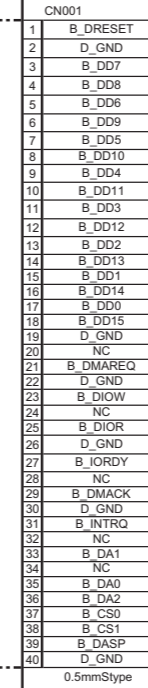
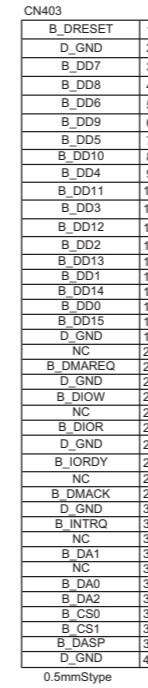


memo

W001 FFC	12	L110
W002 FFC	20	L110
W003 FFC	16	L110
W004 FFC	40	L250
W005 FFC	40	L70
W101 WIRE	09	L300 AWG28
W102 WIRE	06	L100 AWG26
W103 WIRE	04	L380 AWG28
W104 WIRE	04	L260 AWG26
W105 WIRE	04	L190 AWG26
W106 WIRE	02	L50 AWG26



**U001
MAIN**



SCHEMATIC DIAGRAM-1 POWER SUPPLY SECTION

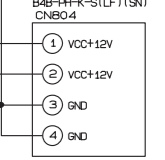
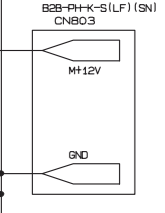
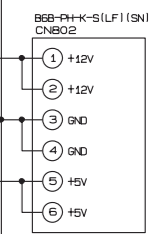
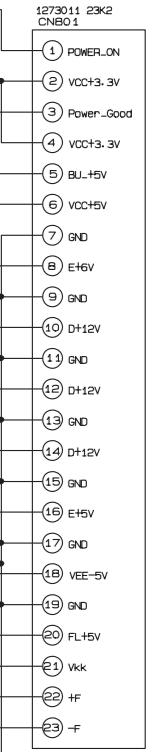
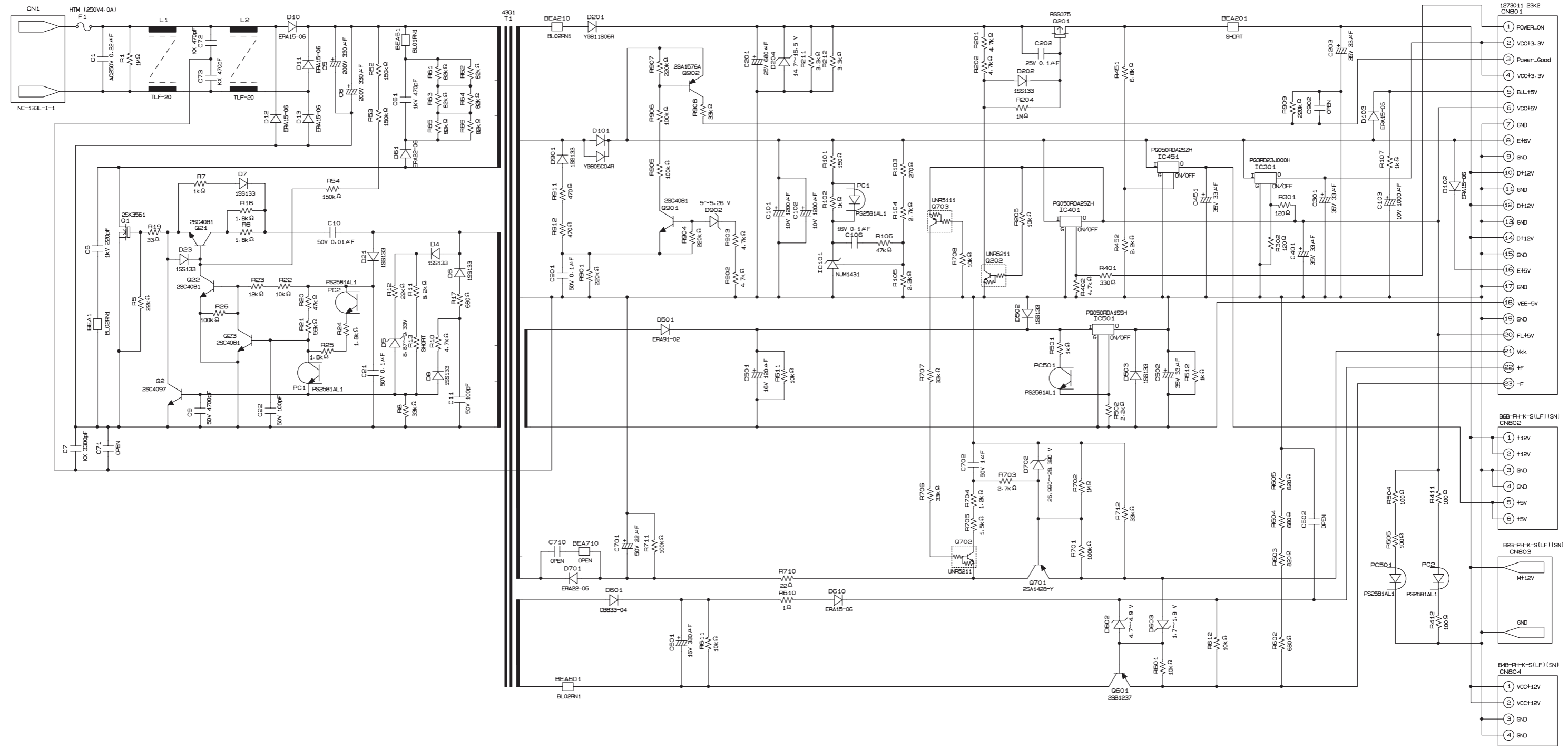
1

2

3

4

5



A

B

C

D

SCHEMATIC DIAGRAM-2 DISPLAY CIRCUIT SECTION

1

2

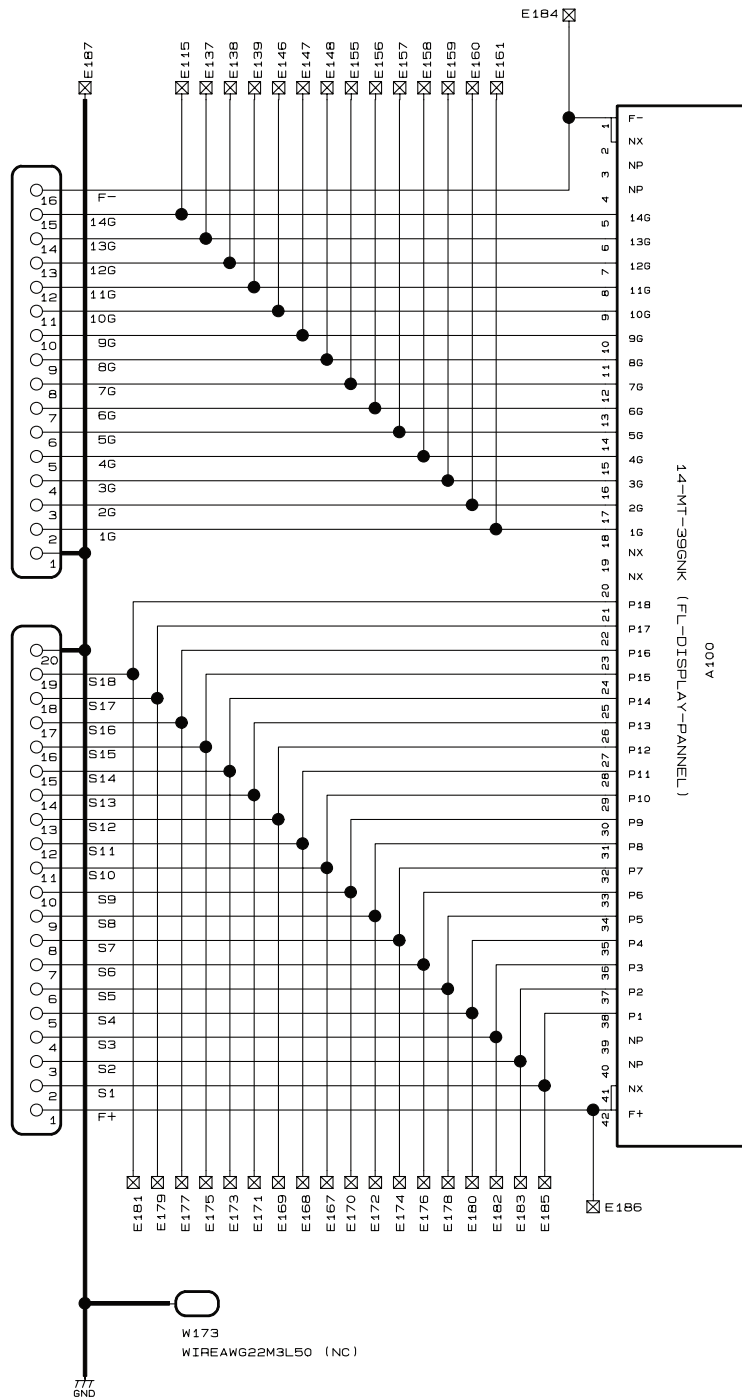
3

4

5

52807-1610
CN104
to MAIN

52807-2010
CN105
to MAIN



A

B

C

D

SCHEMATIC DIAGRAM-3
POWER SWITCH SECTION

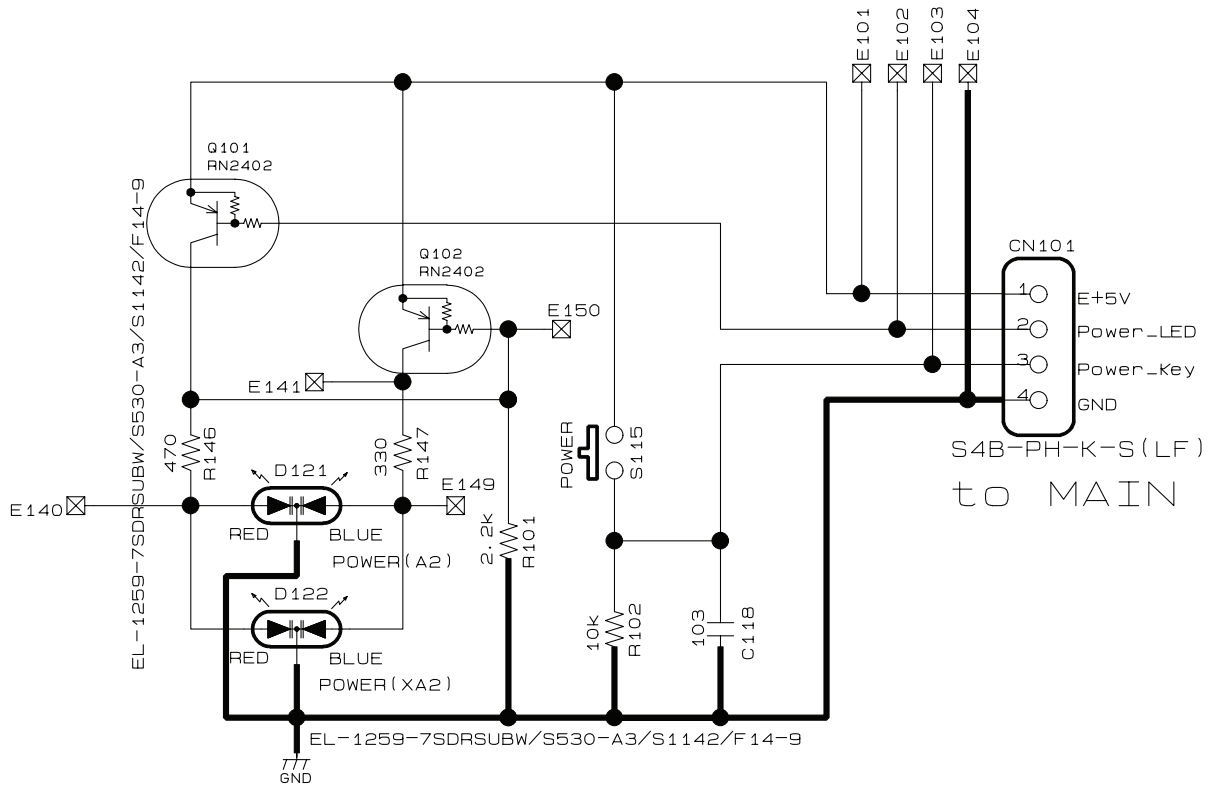
1

2

3

4

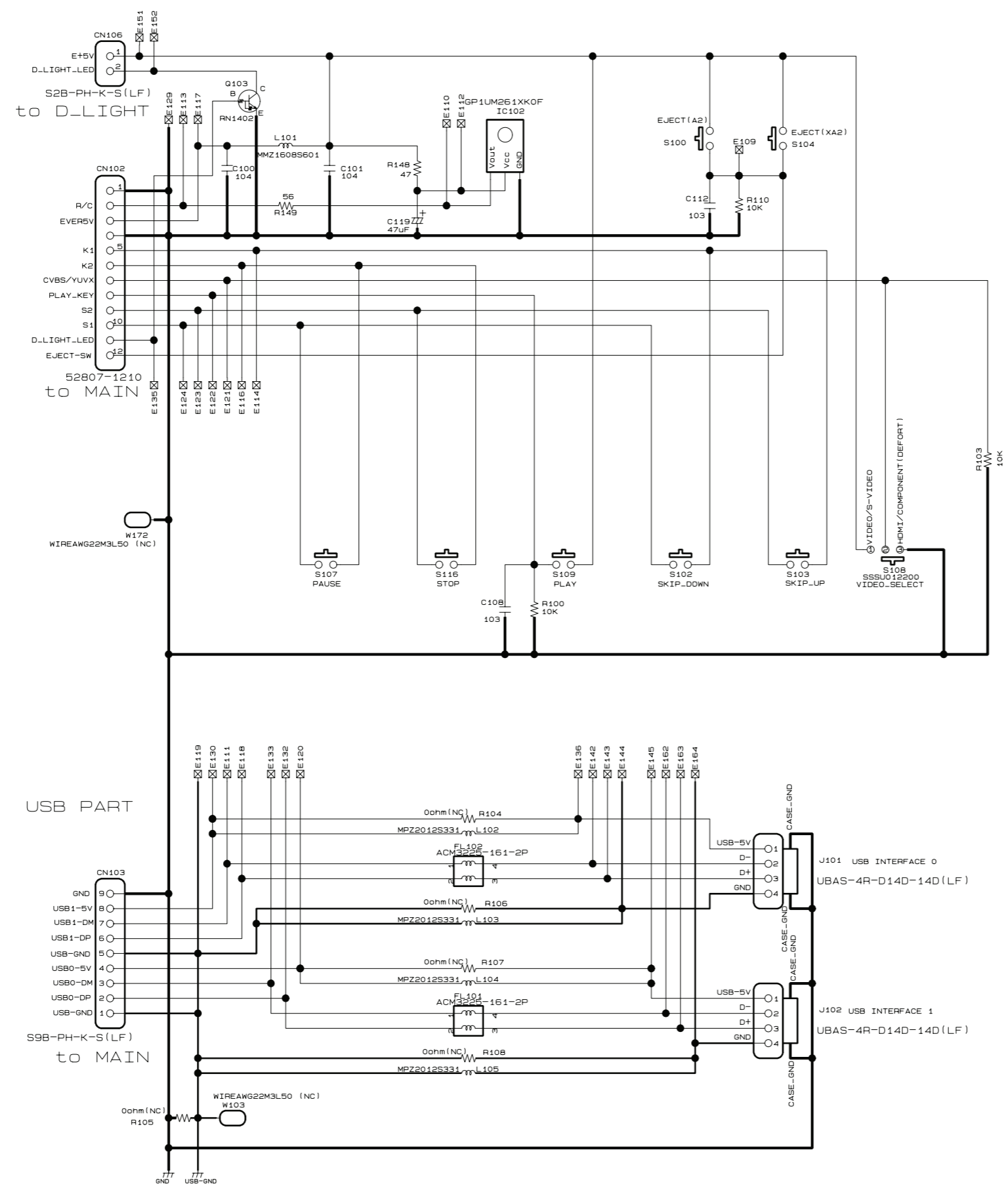
5



D121	×
D122	○

SCHEMATIC DIAGRAM-4 FRONT SWITCH/ USB SECTION

1
2
3
4
5



S100	×
S104	○
S108	○
CN106	○
R100	○
C108	○

A

B

C

D

SCHEMATIC DIAGRAM-5

RS-232C SECTION

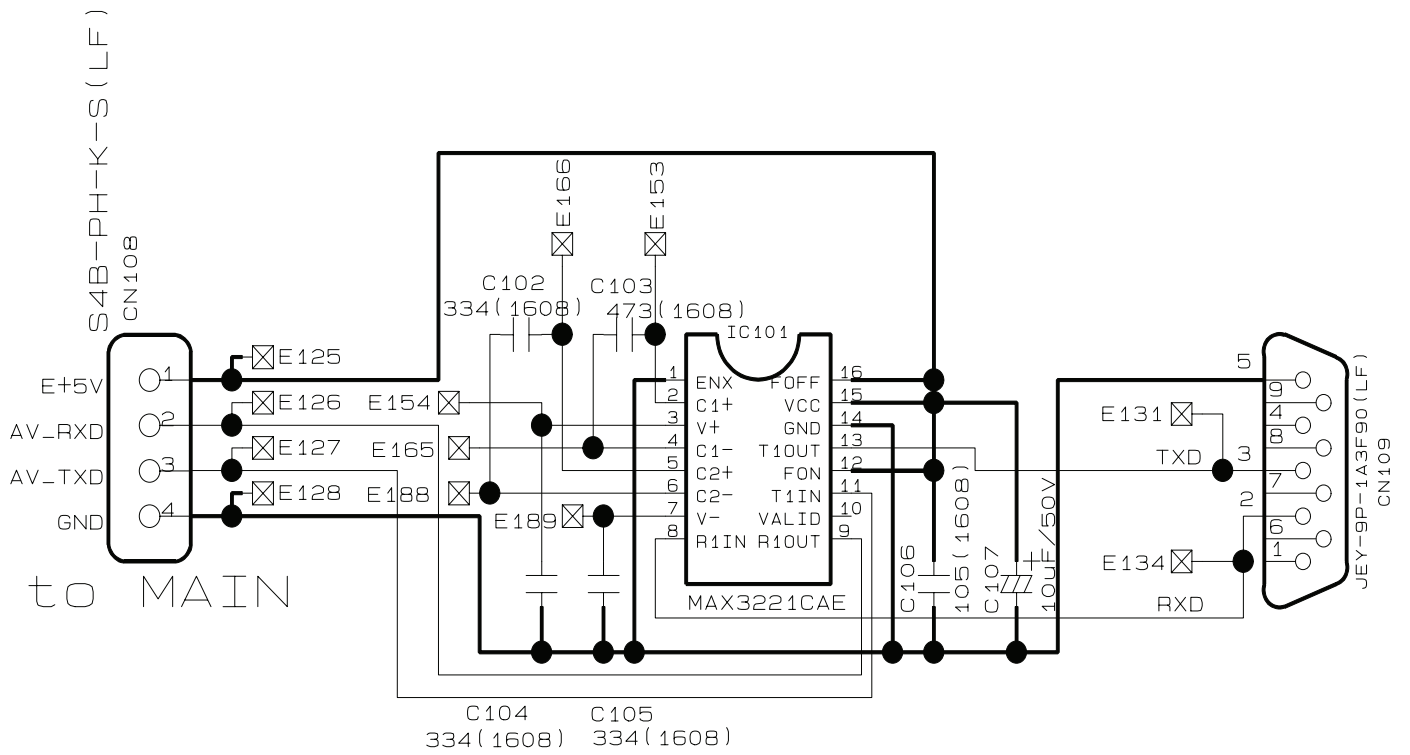
1

2

3

4

5



A

B

C

D

SCHEMATIC DIAGRAM-6

ATAPI SECTION

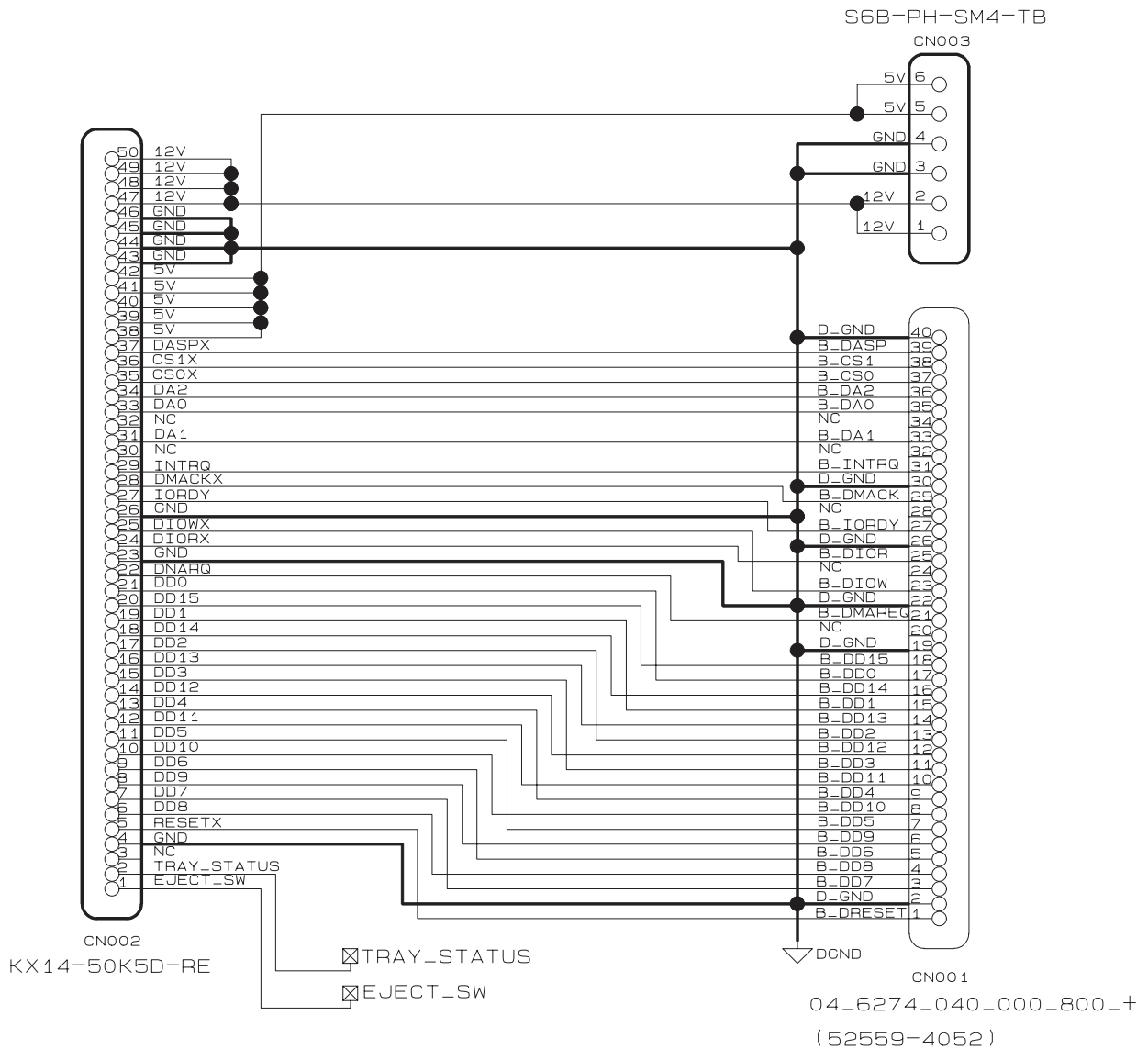
1

2

3

4

5



SCHEMATIC DIAGRAM-8 PC MAIN-2

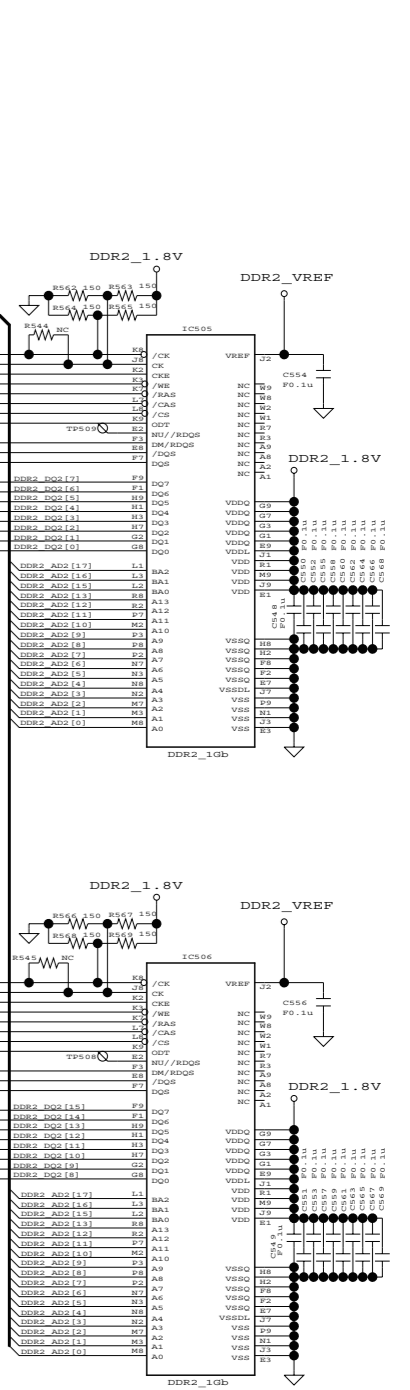
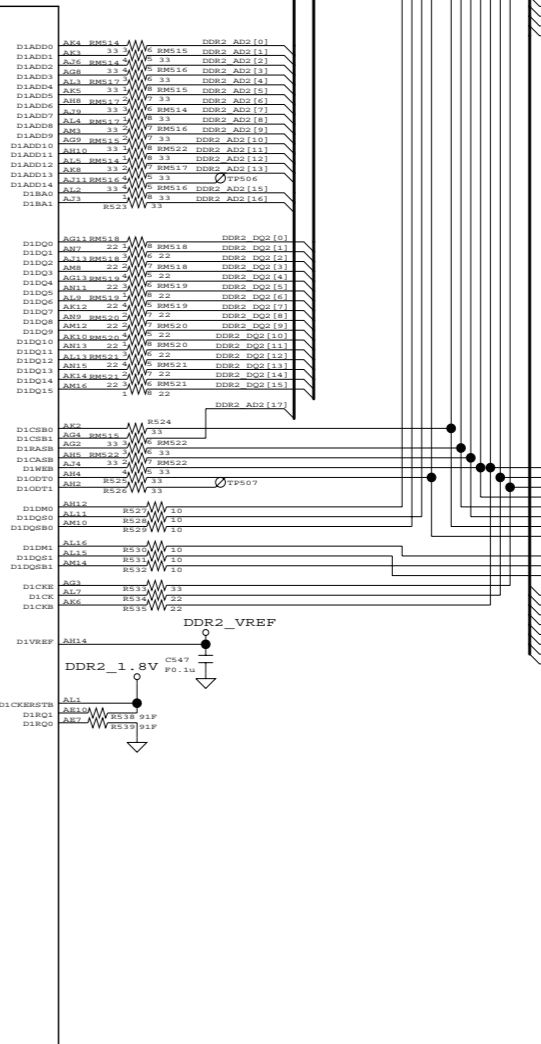
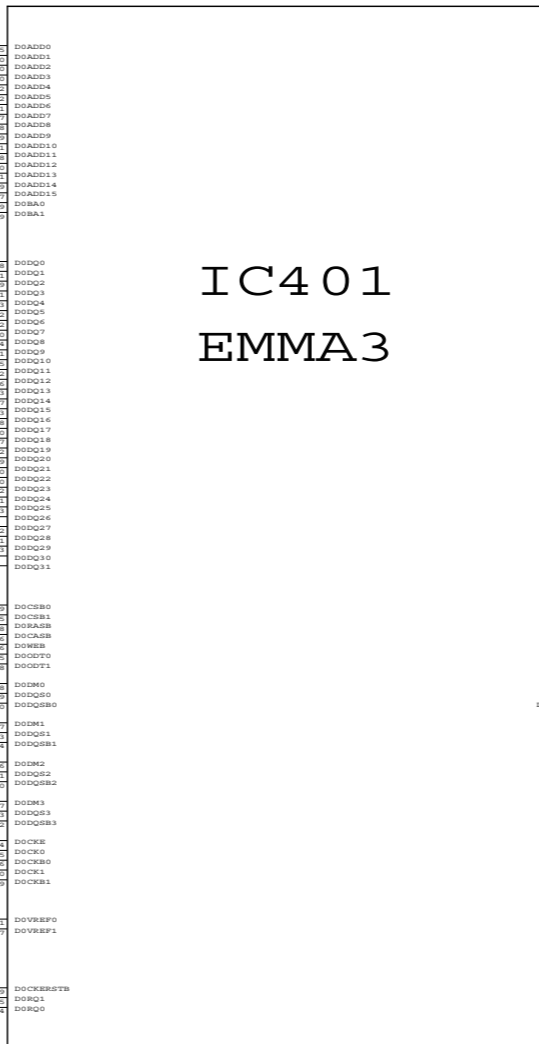
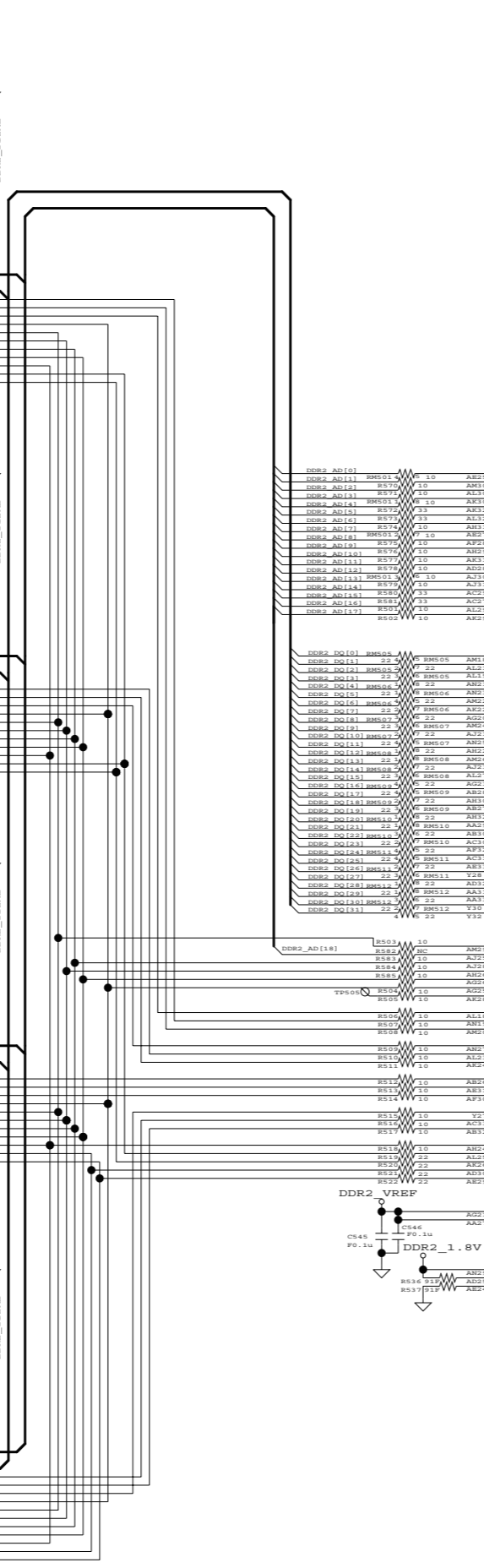
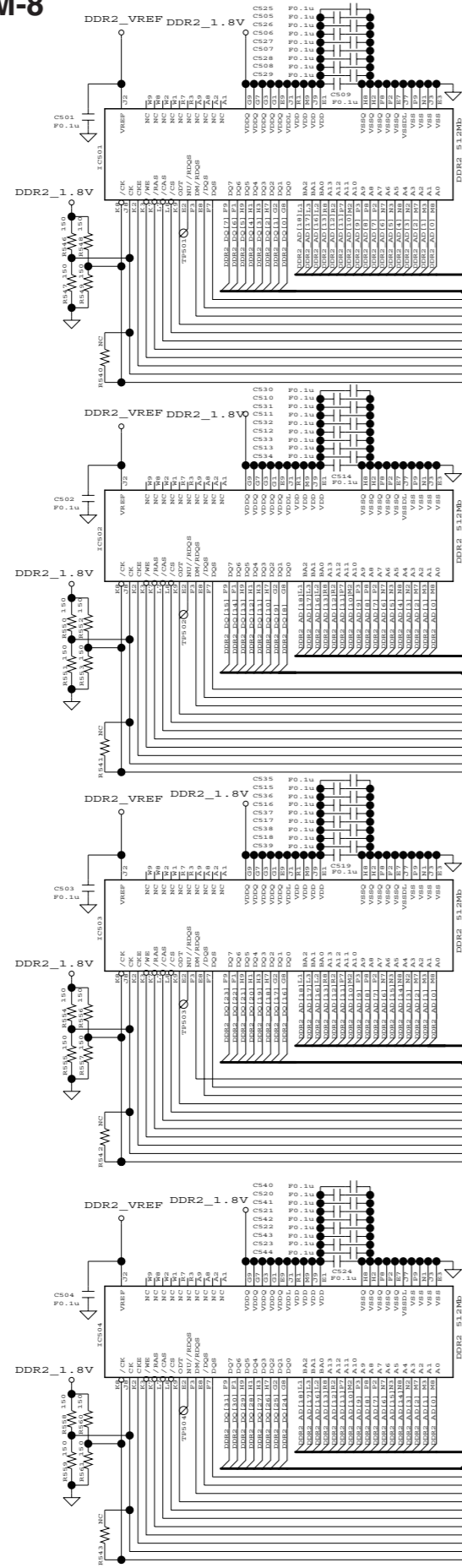
1

2

3

4

5



IC401
EMMA3

IC504

SCHEMATIC DIAGRAM-9 PC MAIN-3

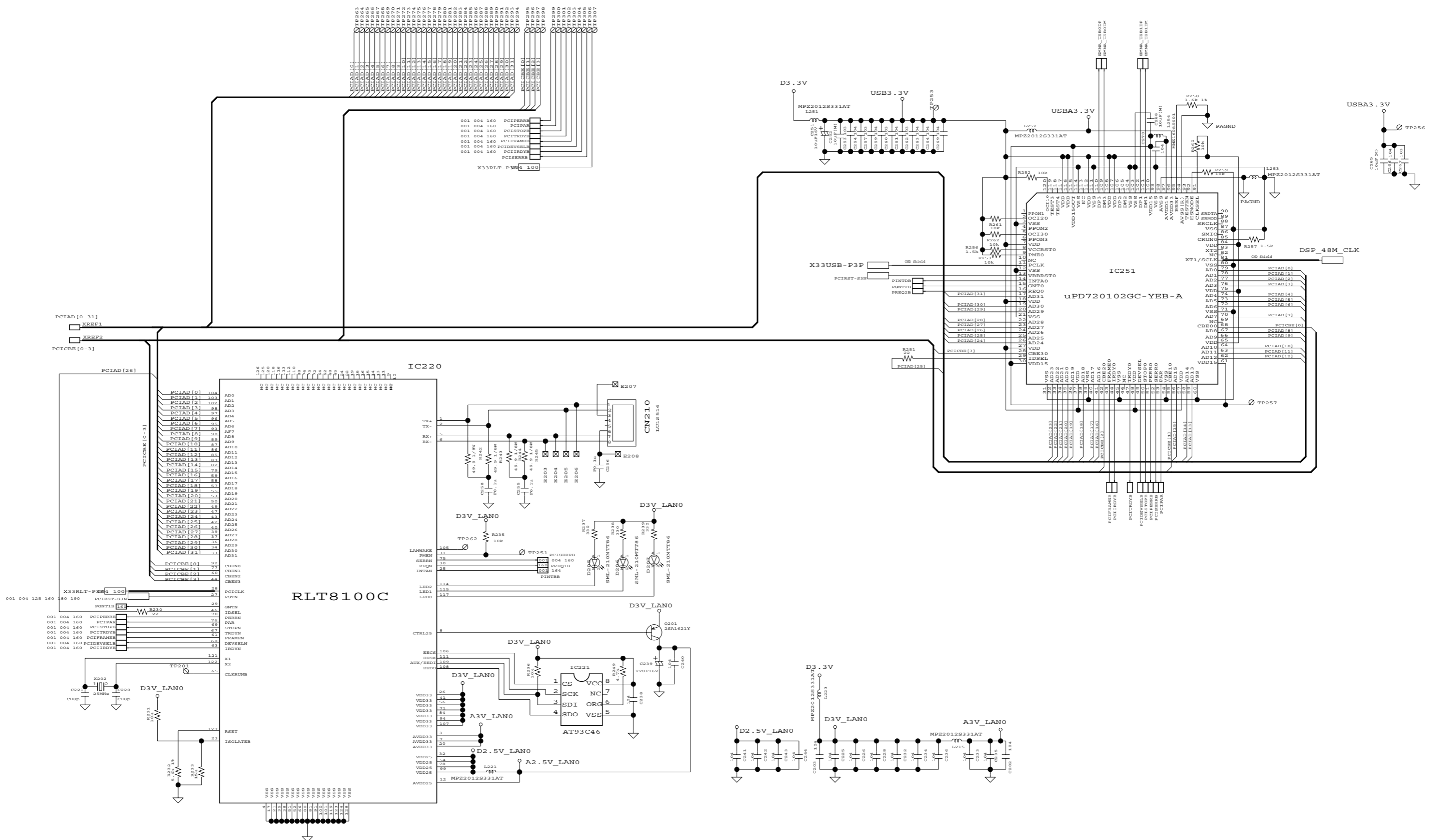
1

2

3

4

5



SCHEMATIC DIAGRAM-10 PC MAIN-4

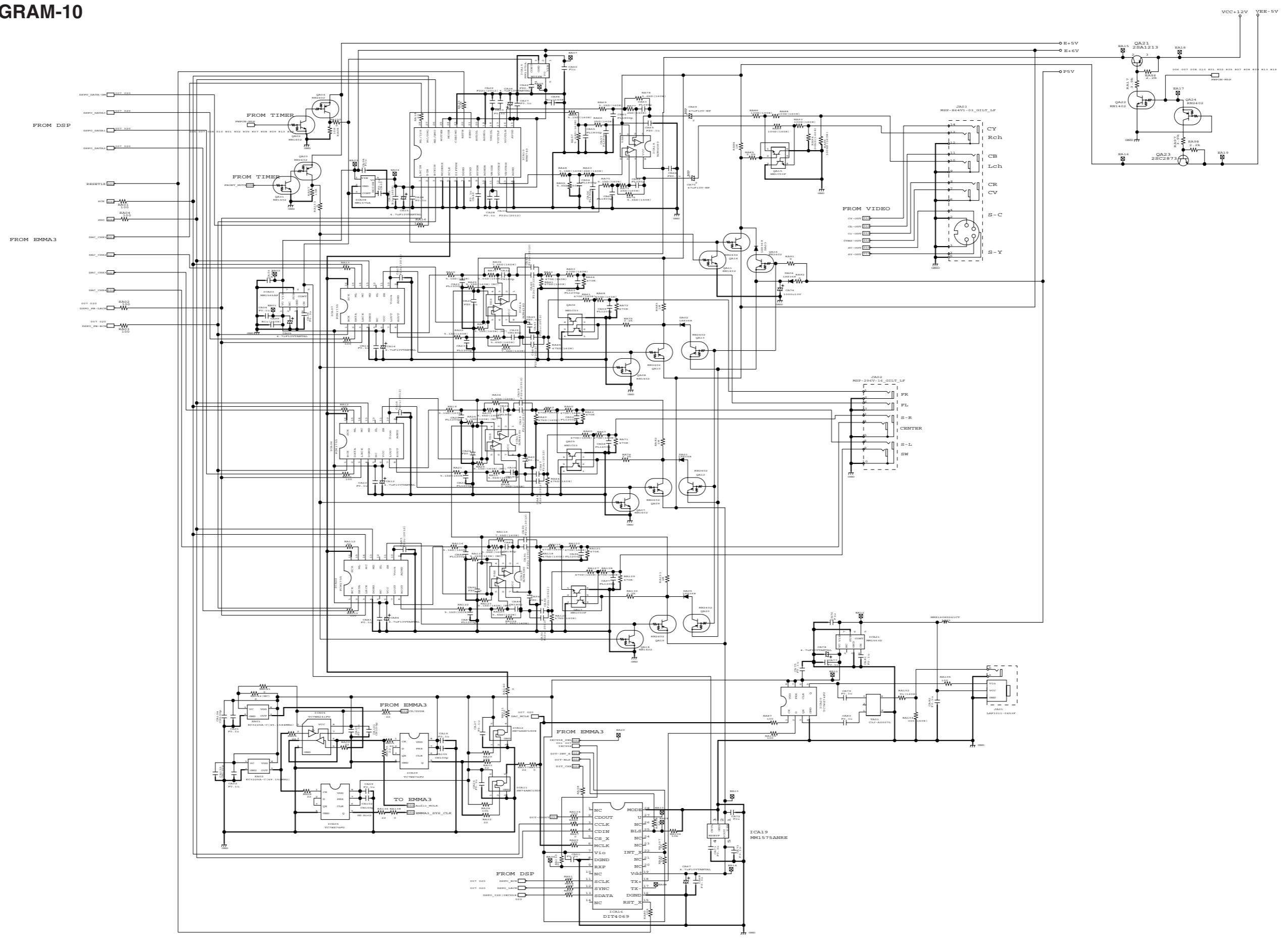
1

2

3

4

5



FROM DSP

FROM EMMA3

FROM VIDEO

FROM TIMER

FROM EMMA3

TO EMMA3

FROM DSP

FROM EMMA3

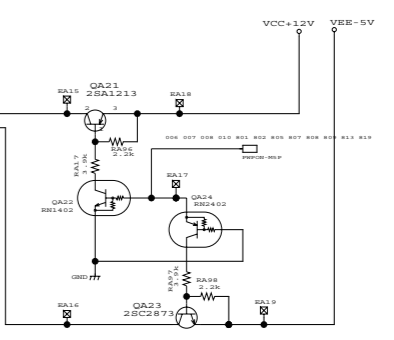
IC19
MM1575ANNE

IC16
DIT4069

IC20
MSP-29EV16_G10V_LP

IC21
MSP-84V1-03_G10V_LP

IC22
MSP-84V1-02_G10V_LP



QA21 2SA1213

QA22 2SC1454

QA23 2SC2873

QA24 2SC2402

RA1 RA2 RA3 RA4 RA5 RA6 RA7 RA8 RA9 RA10

CA1

BR1

T1

CY Rch

CB Lch

CR CV

S-C

S-Y

FR

FL

S-R

S-L

SW

IC20 MSP-29EV16_G10V_LP

IC21 MSP-84V1-03_G10V_LP

IC22 MSP-84V1-02_G10V_LP

RA1 RA2 RA3 RA4 RA5 RA6 RA7 RA8 RA9 RA10

CA1

BR1

T1

CY Rch

CB Lch

CR CV

S-C

S-Y

FR

FL

S-R

S-L

SW

IC20 MSP-29EV16_G10V_LP

IC21 MSP-84V1-03_G10V_LP

IC22 MSP-84V1-02_G10V_LP

RA1 RA2 RA3 RA4 RA5 RA6 RA7 RA8 RA9 RA10

CA1

BR1

T1

SCHEMATIC DIAGRAM-11

PC MAIN-5

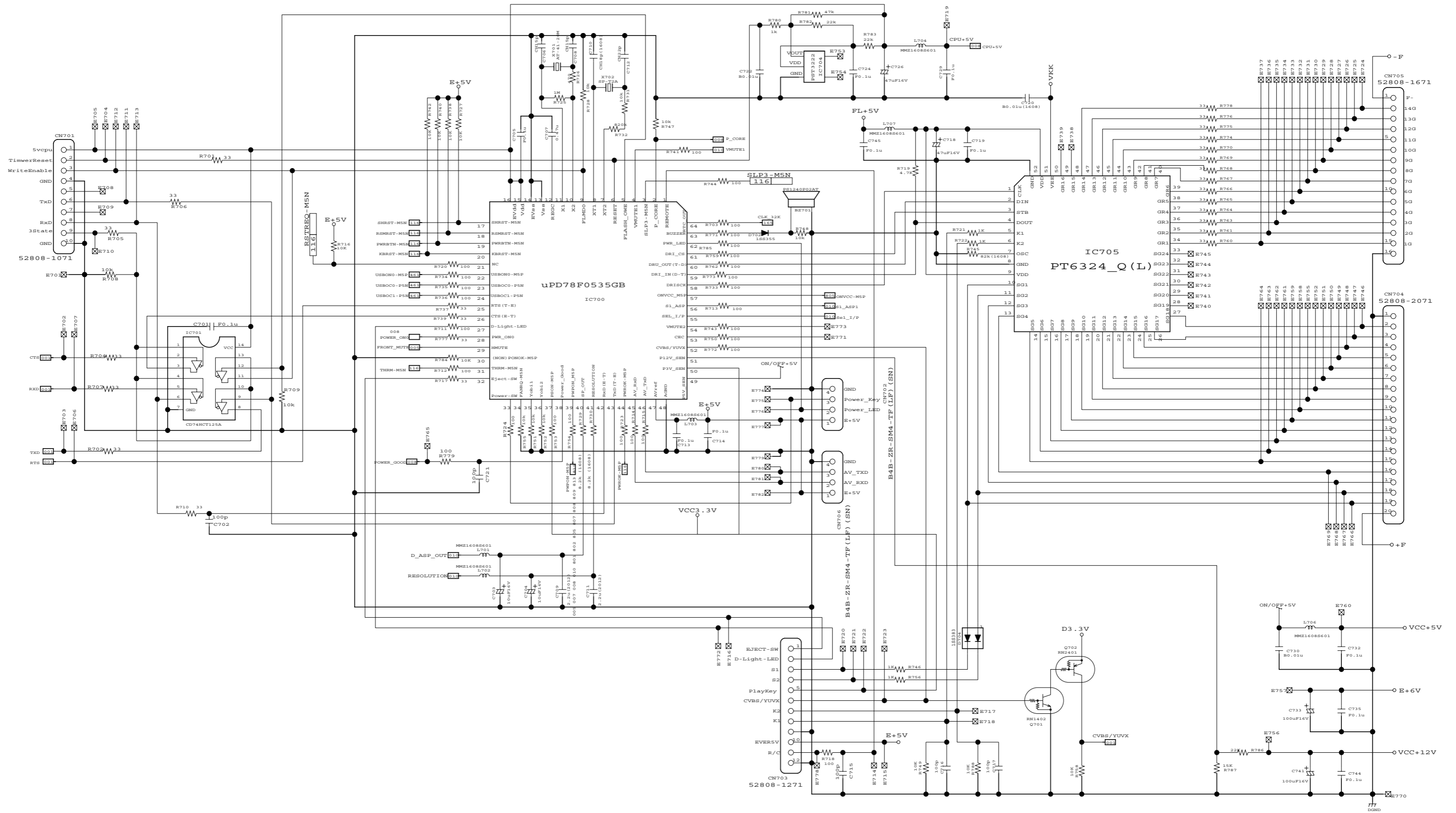
1

2

3

4

5



SCHEMATIC DIAGRAM-12
PC MAIN-6

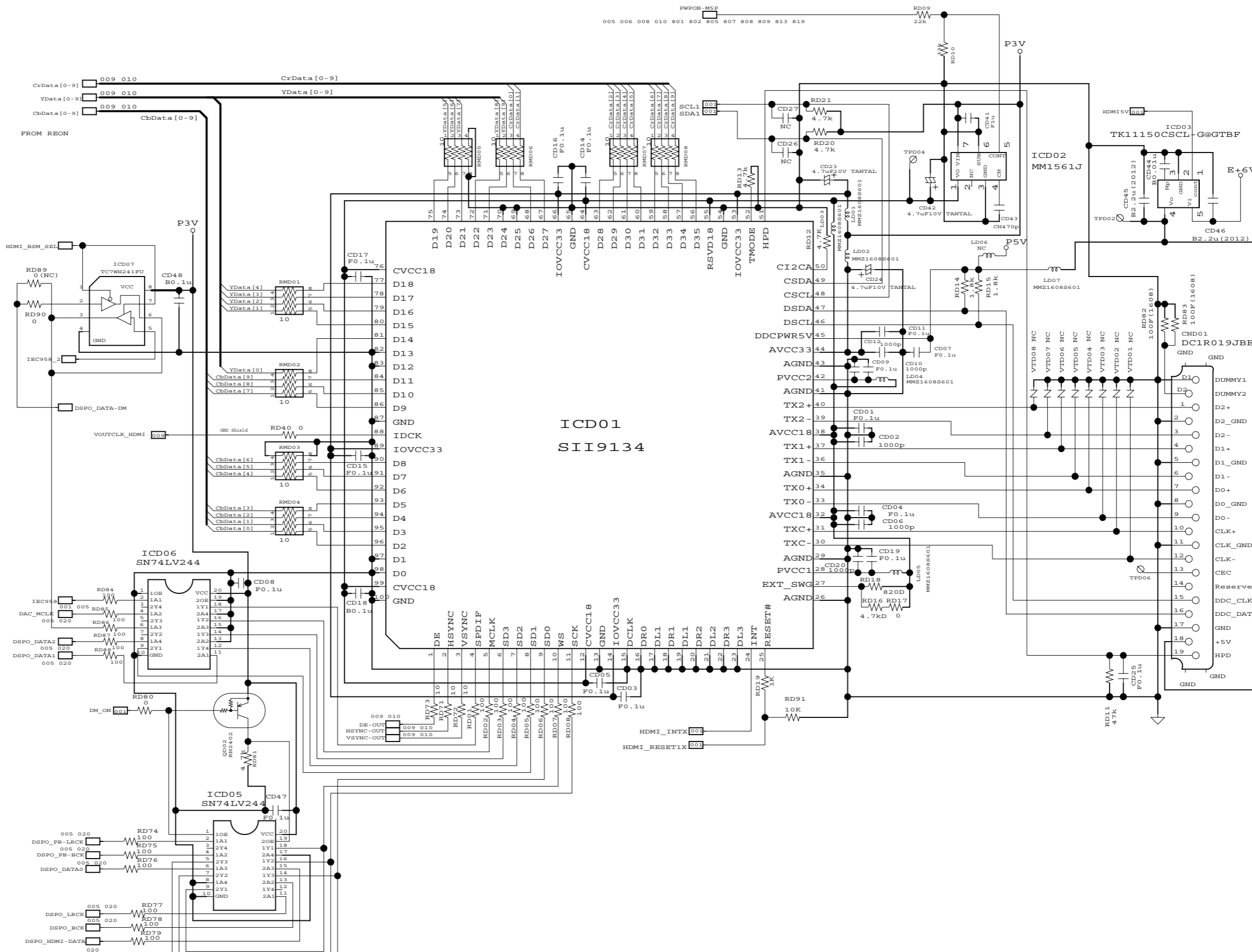
1

2

3

4

5



SCHEMATIC DIAGRAM-14 PC MAIN-8

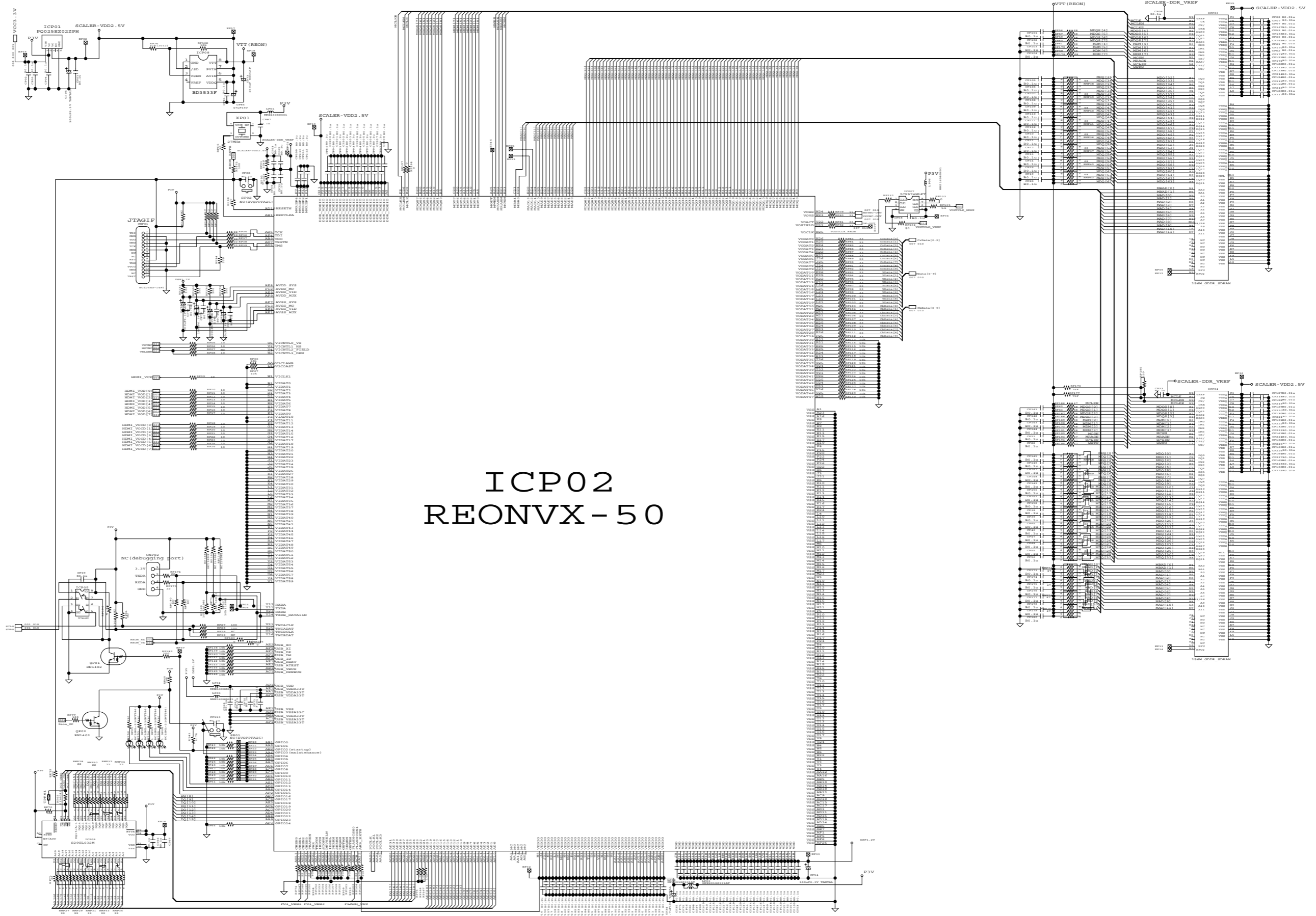
1

2

3

4

5



ICP02 REONVX-50

SCHEMATIC DIAGRAM-15 PC MAIN-9

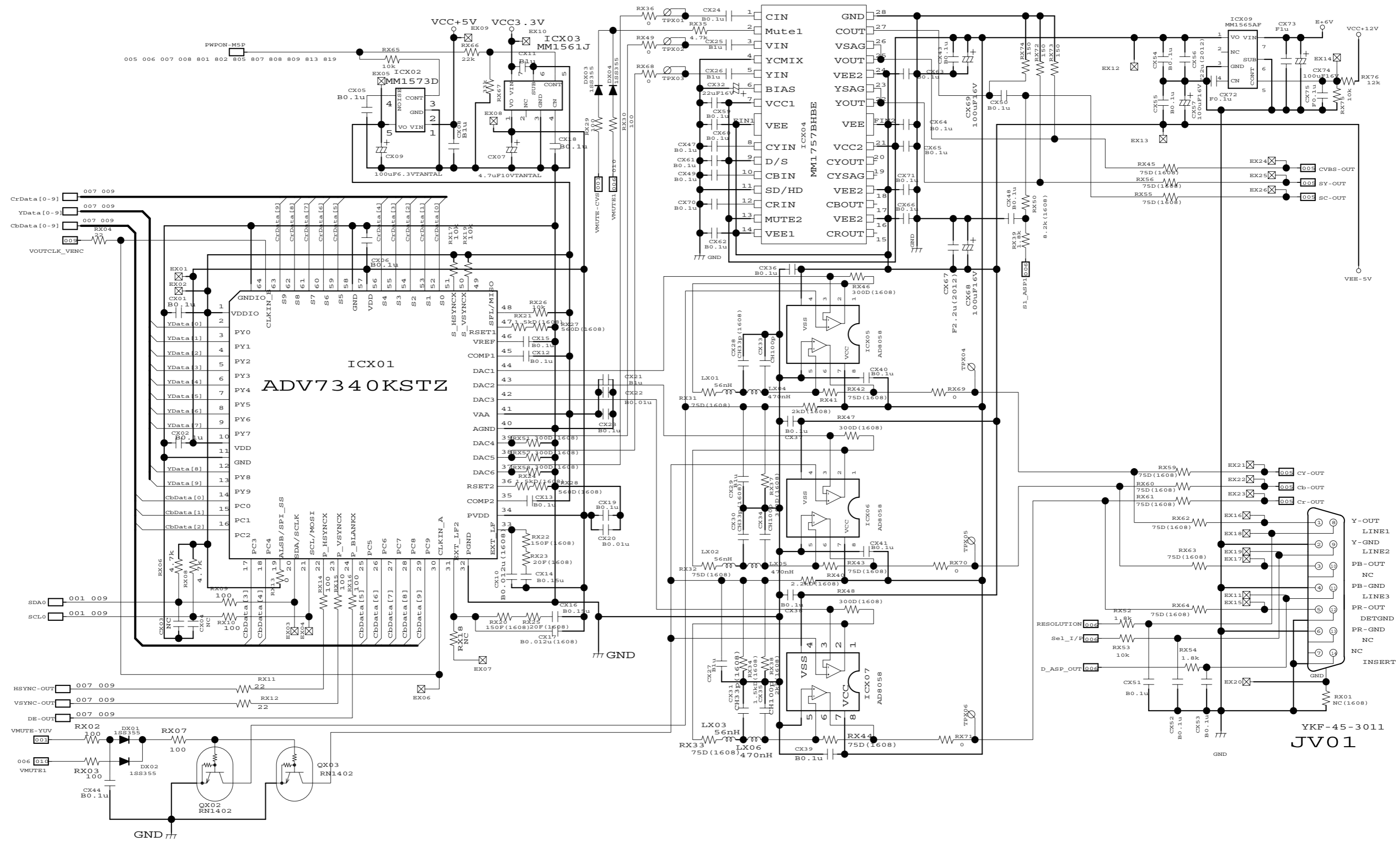
1

2

3

4

5



YKF-45-3011
JVO1

- Y-OUT
- LINE1
- Y-GND
- LINE2
- PB-OUT
- NC
- PB-GND
- LINE3
- PR-OUT
- DETGND
- PR-GND
- NC
- NC
- INSERT

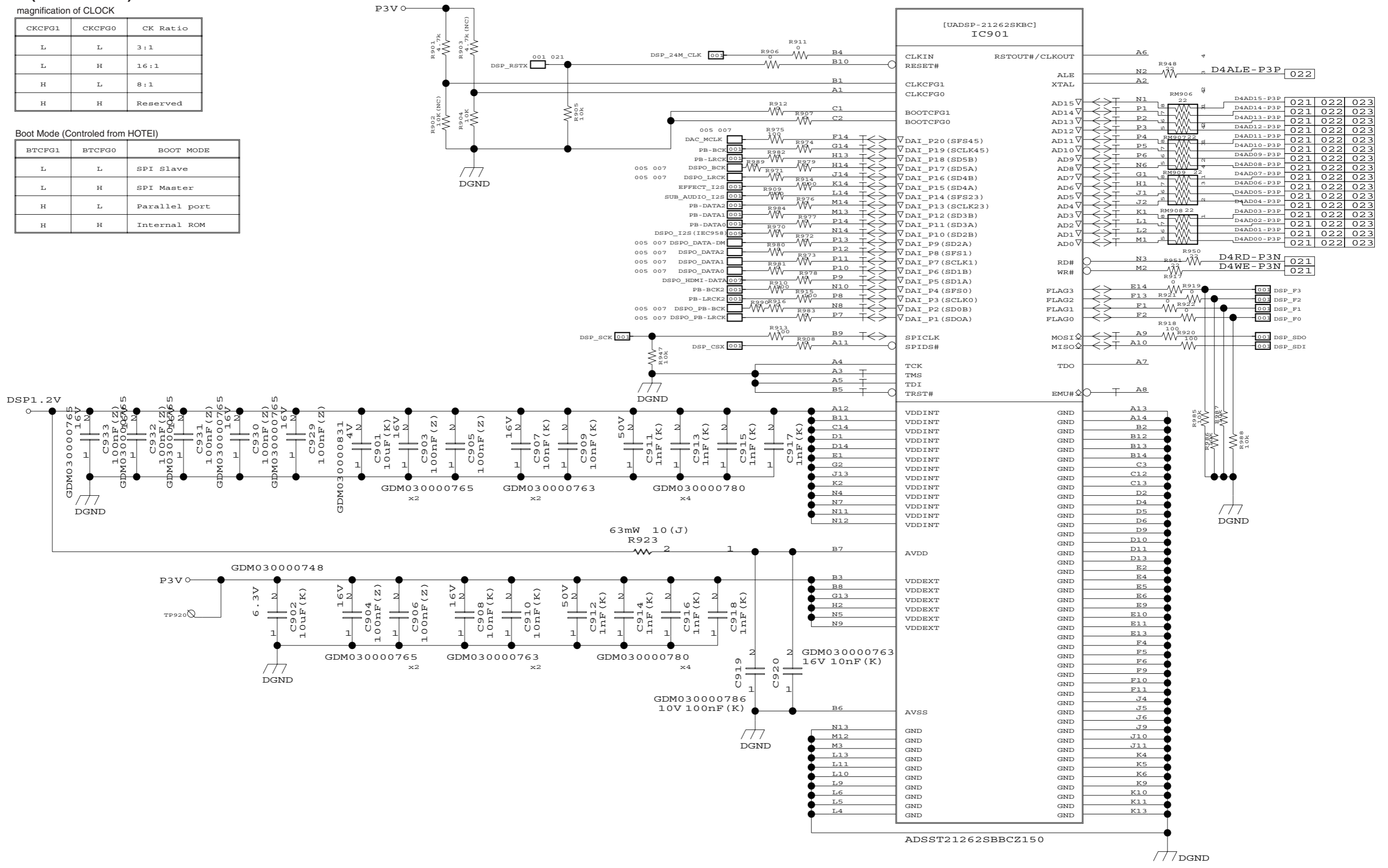
SCHEMATIC DIAGRAM-16
DSP SECTION (ADSP-21262)

magnification of CLOCK

CKCFG1	CKCFG0	CK Ratio
L	L	3:1
L	H	16:1
H	L	8:1
H	H	Reserved

Boot Mode (Controlled from HOTEL)

BTCFG1	BTCFG0	BOOT MODE
L	L	SPI Slave
L	H	SPI Master
H	L	Parallel port
H	H	Internal ROM



1

2

3

4

5

SCHEMATIC DIAGRAM-17 DSP SECTION (RAM & FROM)

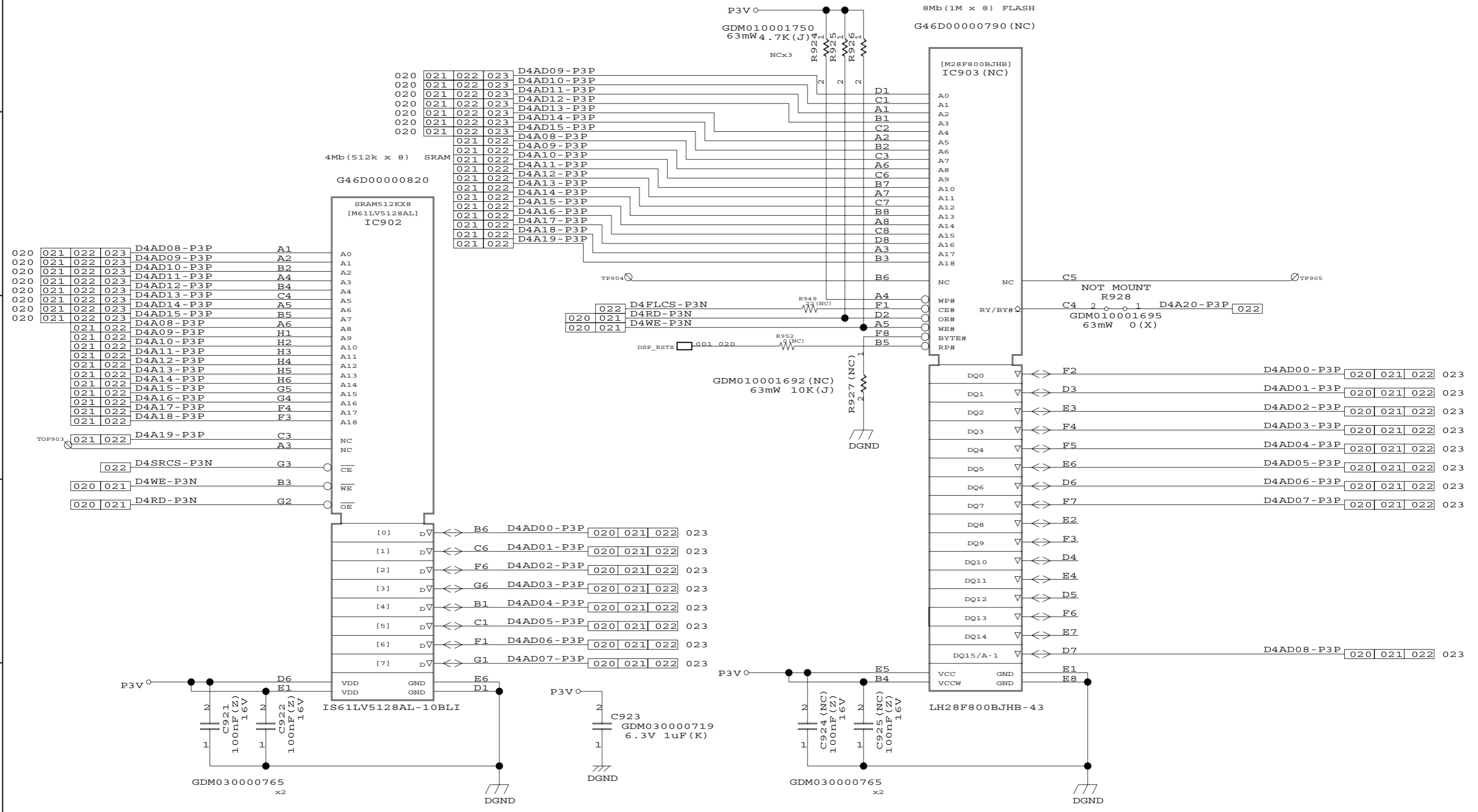
1

2

3

4

5



SCHEMATIC DIAGRAM-18
DSP SECTION (ADDRESS LATCH)

1

2

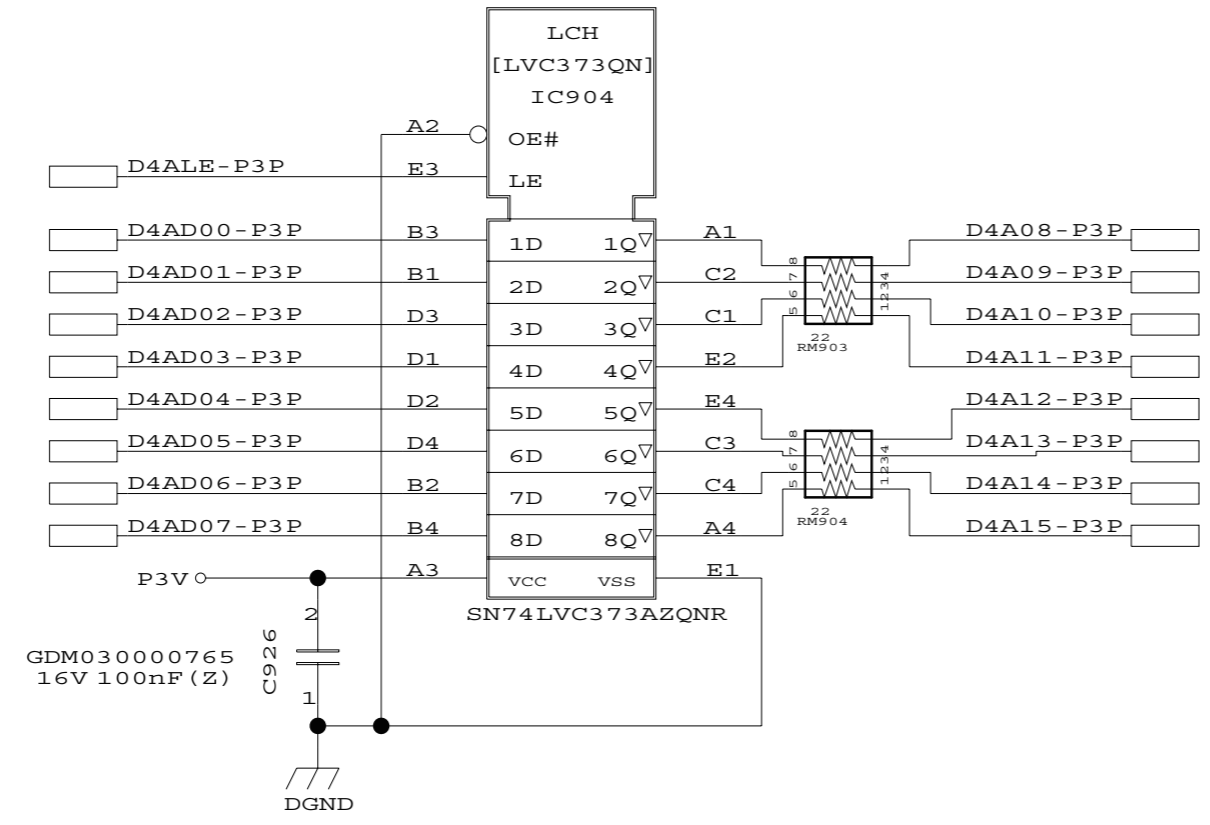
3

4

5

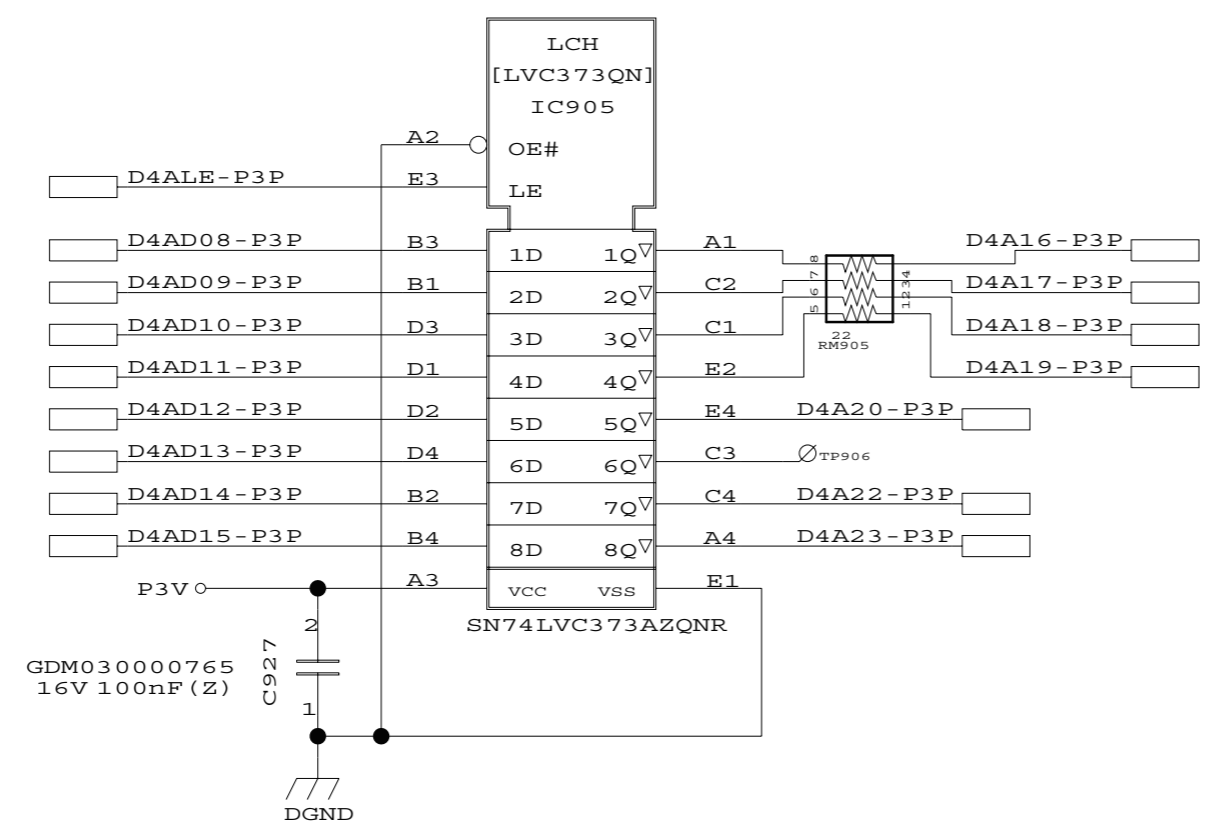
Address Latch
G45D00000320

DSP ADDR LATCH

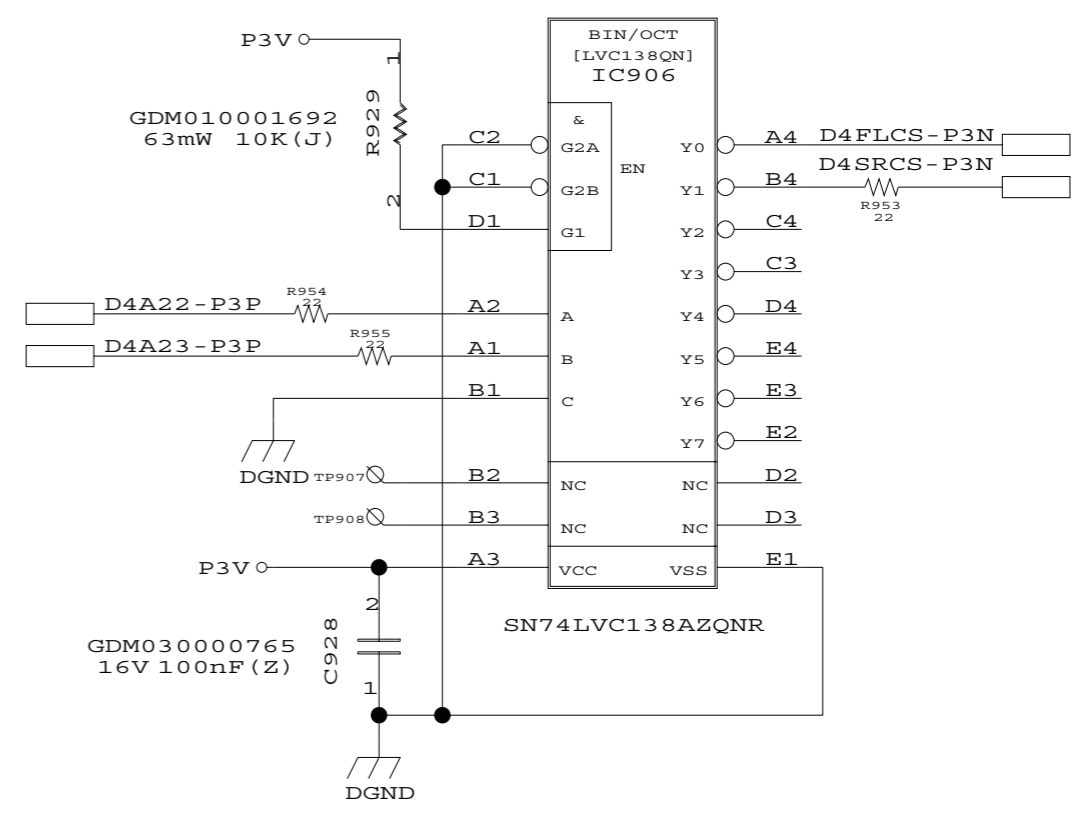


Valid DSP Address		BANK END Address	A23	A22	BANK	Device
Start	End					
80 0000	X	FF FFFF	-	-	-	None
40 0000	47 FFFF	7F FFFF	0	0	Y1	SRAM
00 0000	0F FFFF	3F FFFF	0	0	Y0	FLASH

G45D00000320



Address Decoder
G45D00000330



A

B

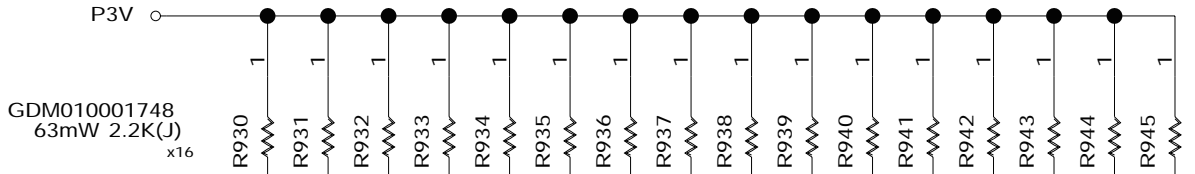
C

D

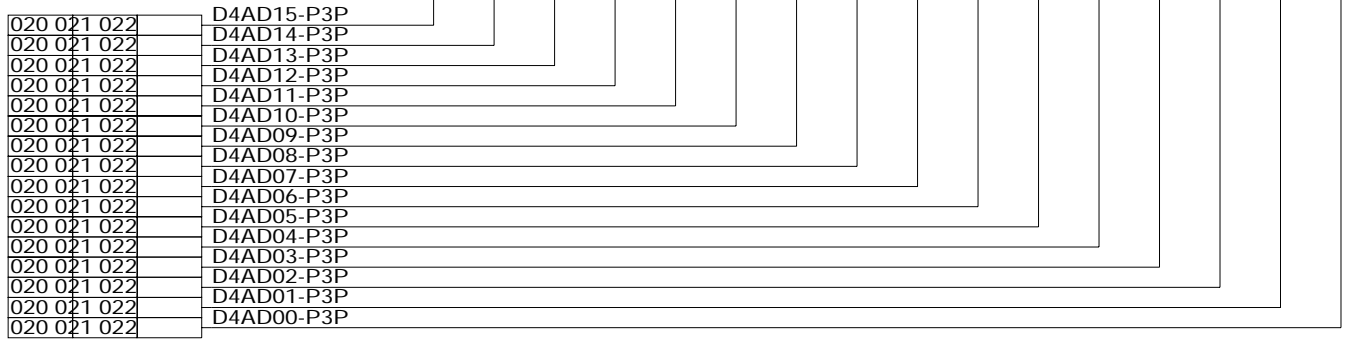
SCHEMATIC DIAGRAM-19

DSP SECTION (PULL UP)

1

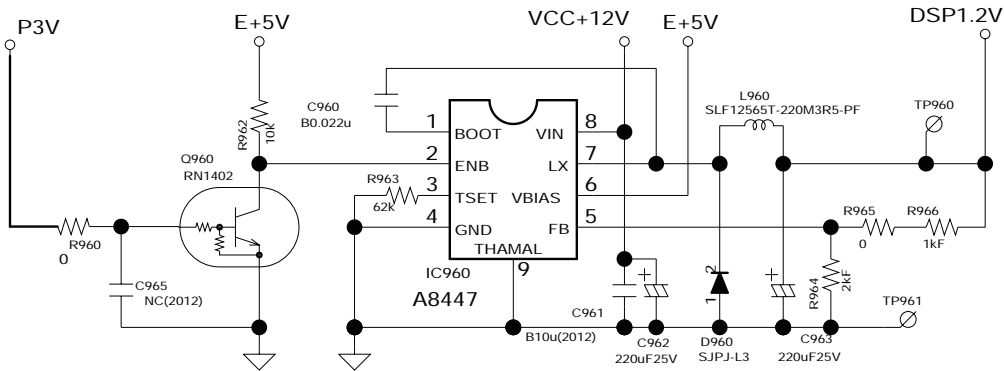


2



3

4



5

SCHEMATIC DIAGRAM-20 DSP SECTION (CK408)

FS [210]	CPUCLK	BSEL [10]	CPUCLK
000	66	00	(100MHz)
001	100	01	133MHz
010	200	10	(200MHz)
011	133	11	RESERVED

CK408

CPUCLK	2.0-8.5inch
CLK66	4.0-9.0inch

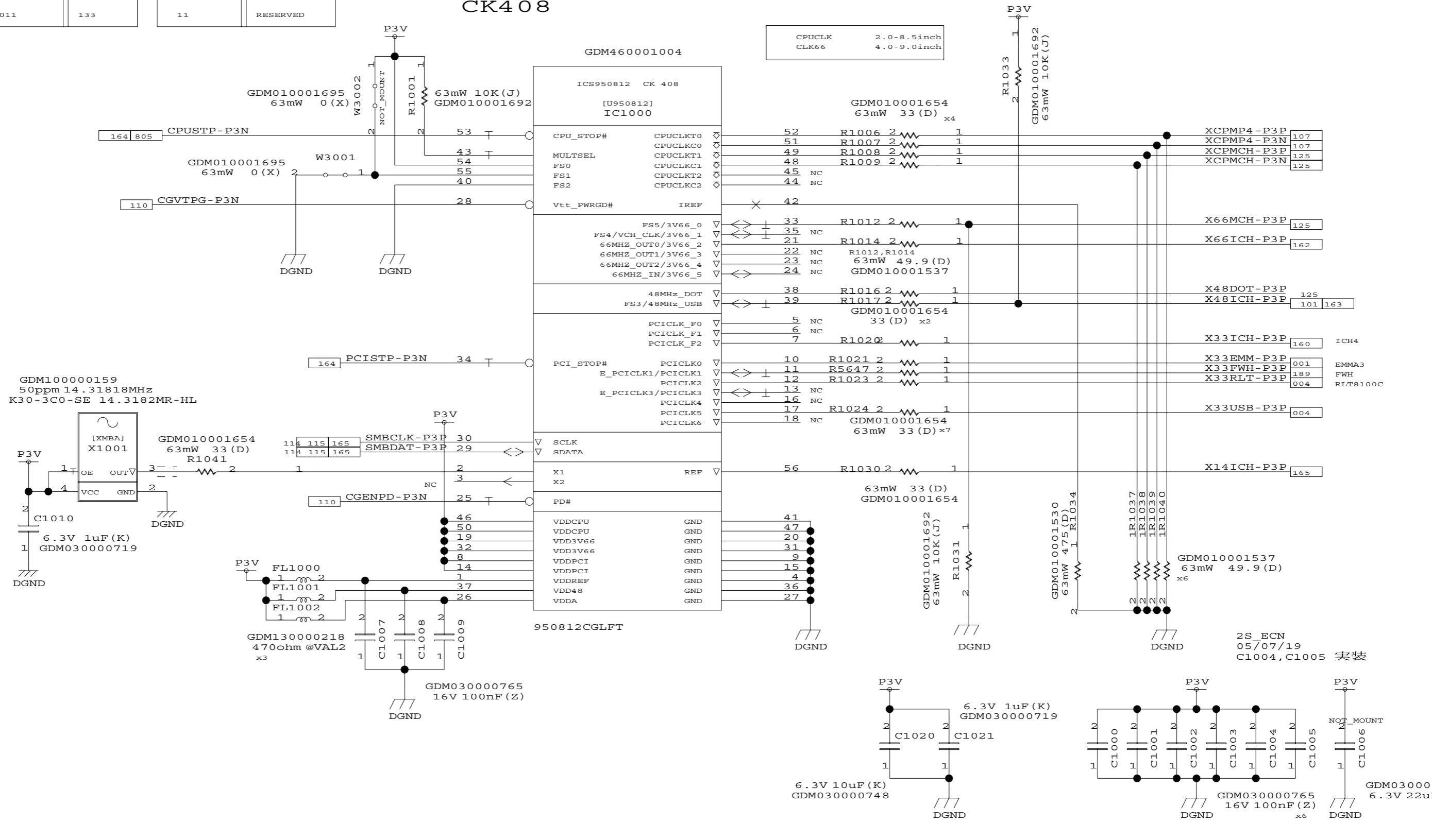
1

2

3

4

5



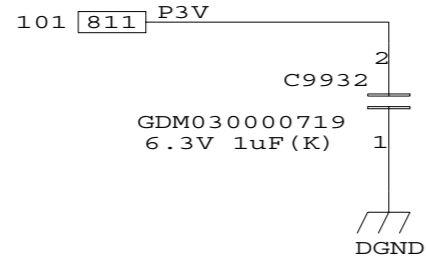
2S_ECN
05/07/19
C1004, C1005 実装

GDM030000758
6.3V 22uF (K)

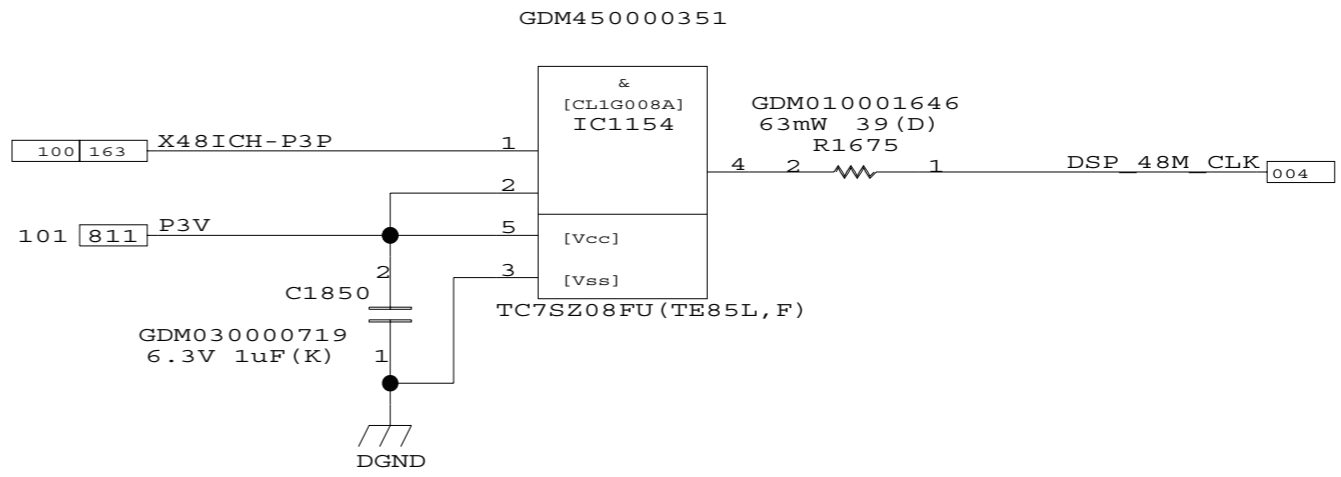
A B C D E F G H

SCHEMATIC DIAGRAM-21
X48 BRANCH SECTION

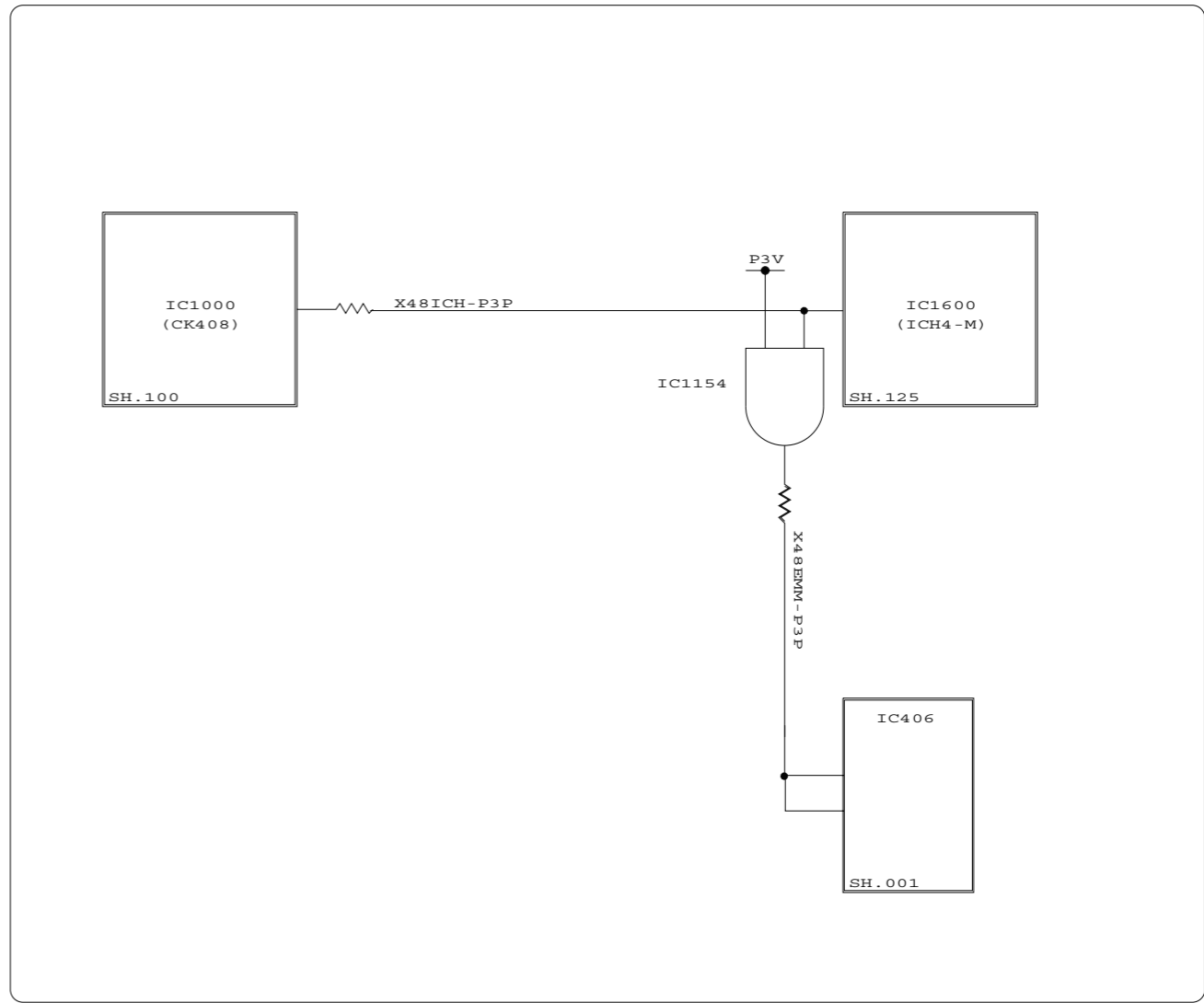
1



2



3



4

5

A

B

C

D

E

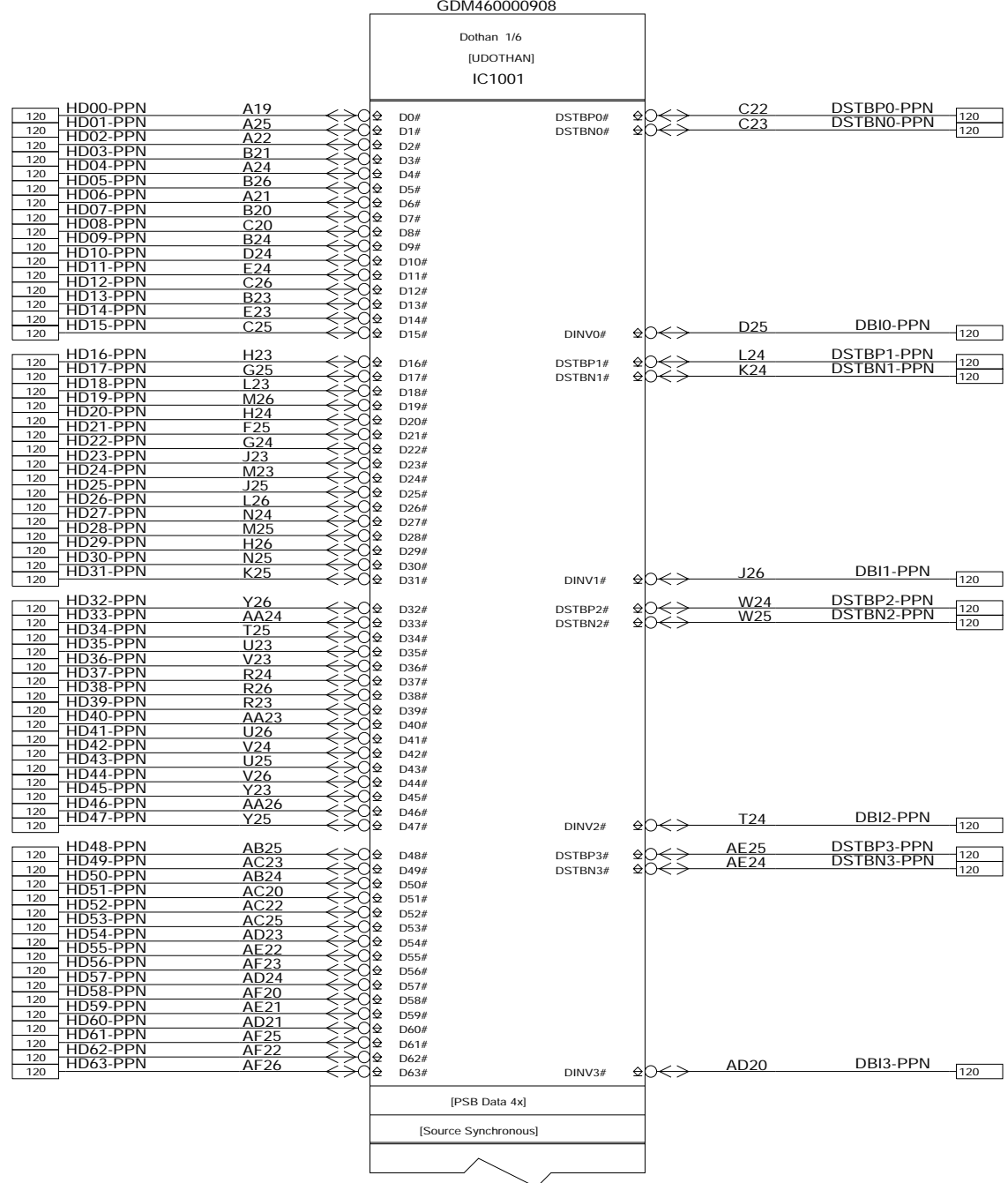
SCHEMATIC DIAGRAM-22
ULV CELELON-M1

1

2

3

4



SCHEMATIC DIAGRAM-23
ULV CELERON-M2

1

2

3

4

A

B

C

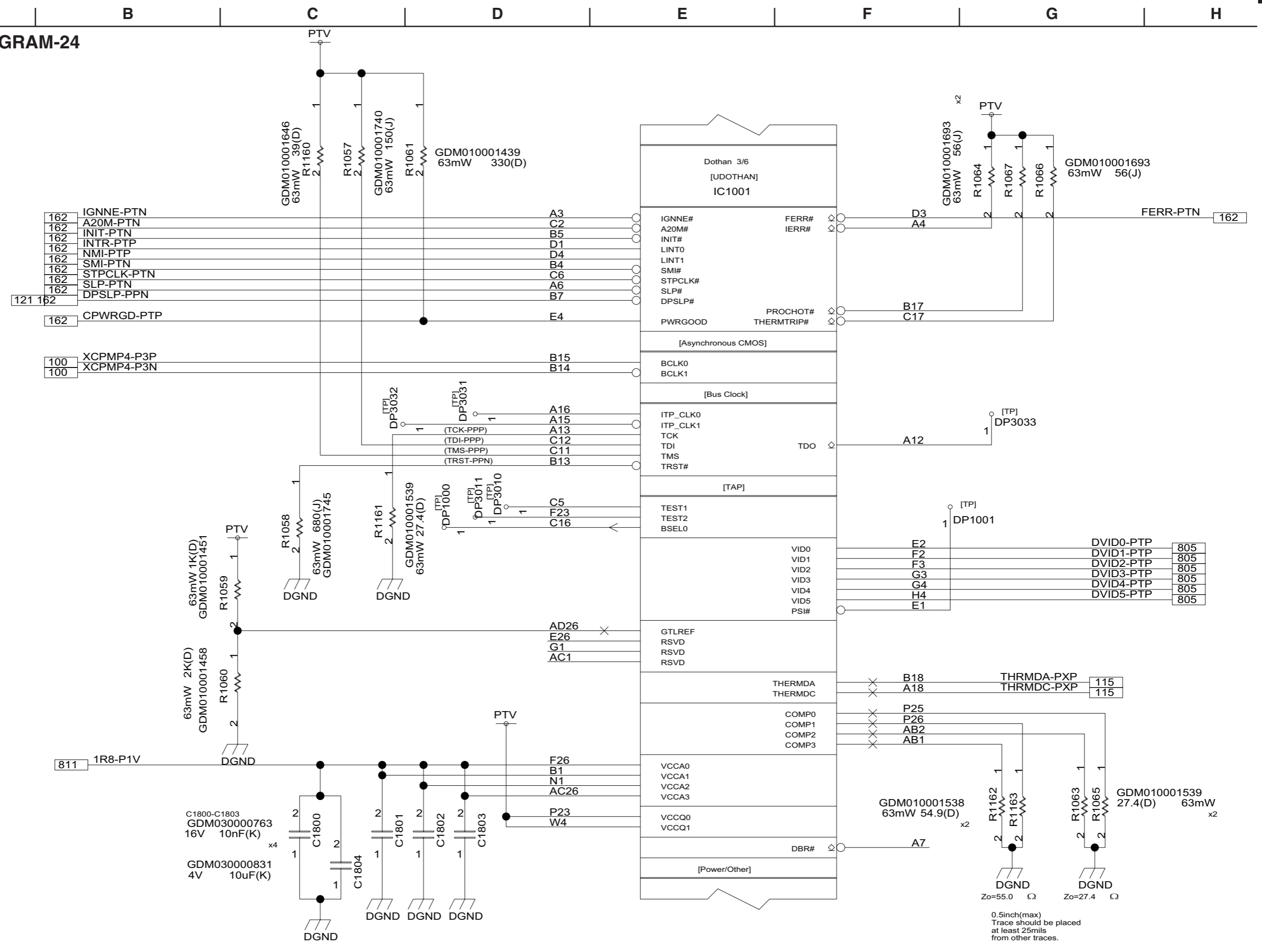
D

E



SCHEMATIC DIAGRAM-24 ULV CELERON-M3

1
2
3
4
5



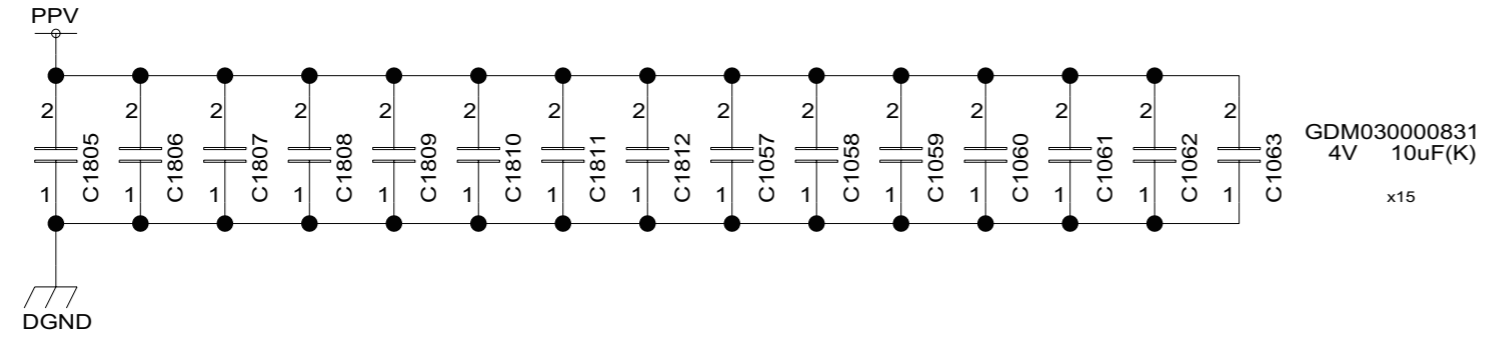
0.5inch(max)
Trace should be placed
at least 25mils
from other traces.

A B C D E F G H

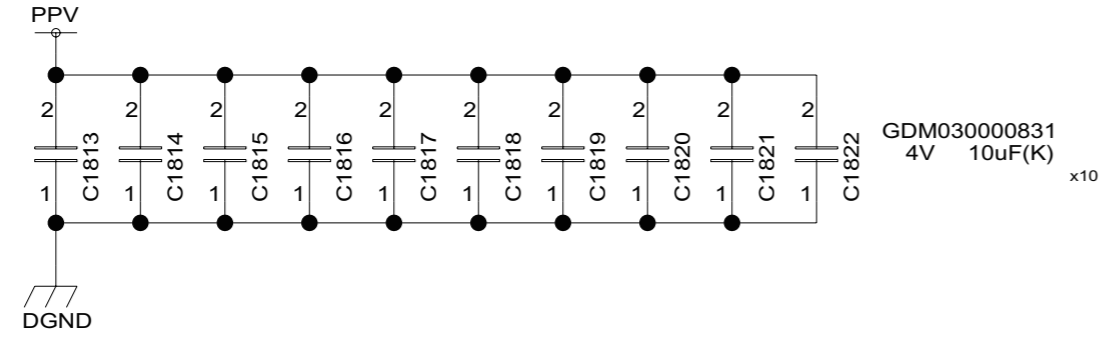
SCHEMATIC DIAGRAM-25

ULV SELERON-M4

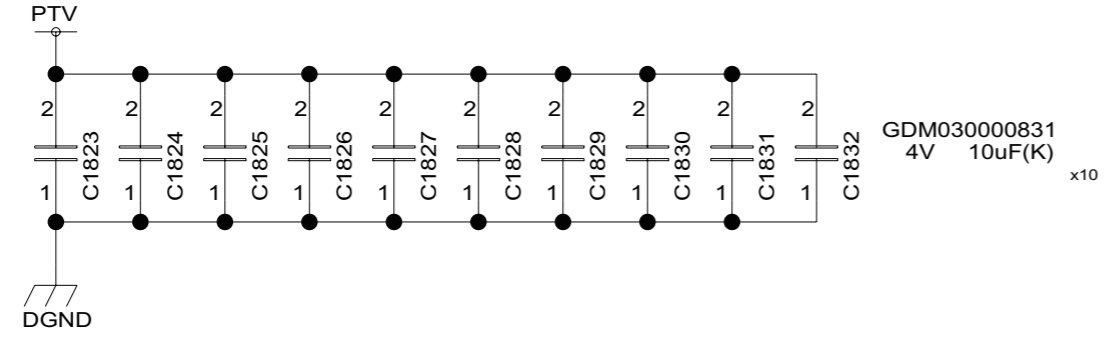
1



2

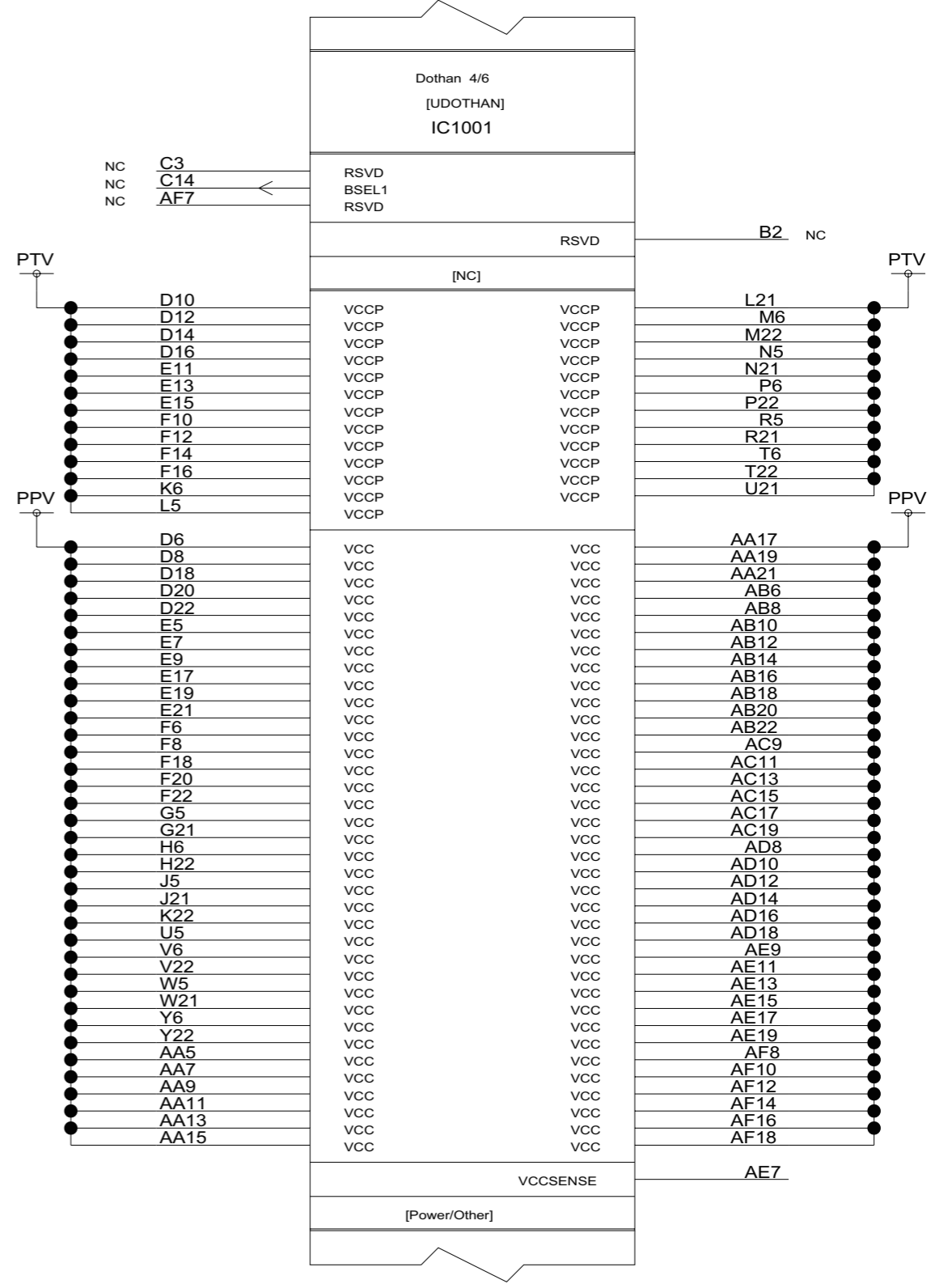


3

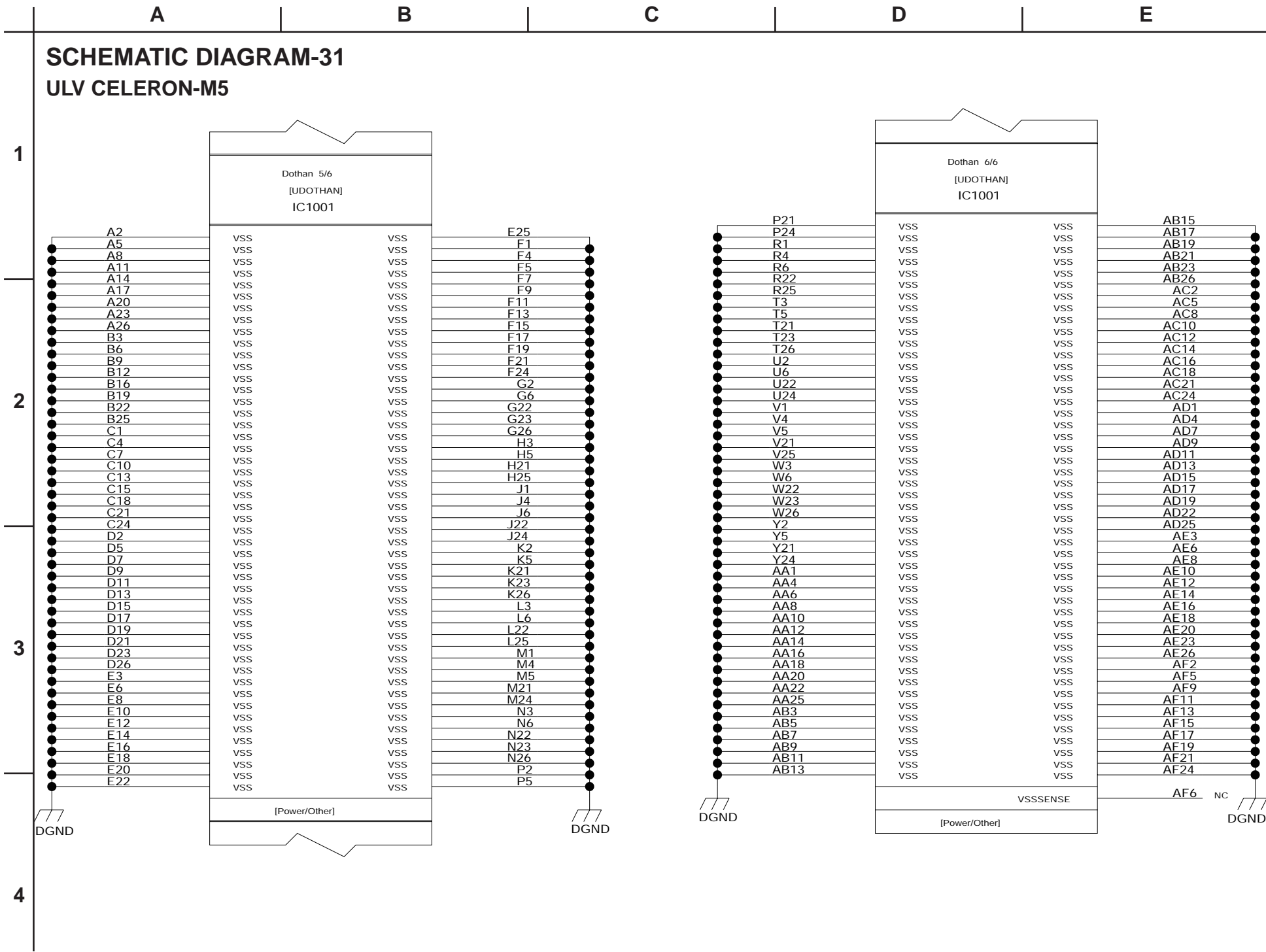


4

5



SCHEMATIC DIAGRAM-31
ULV CELERON-M5



A

B

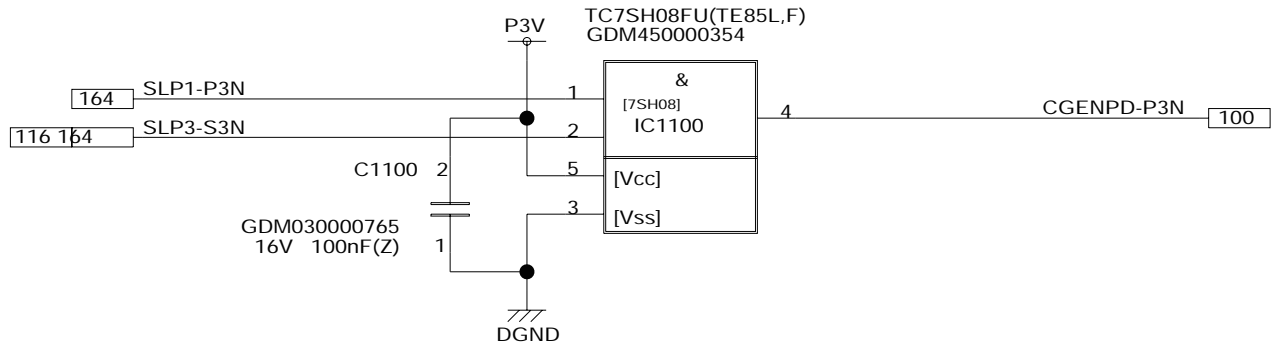
C

D

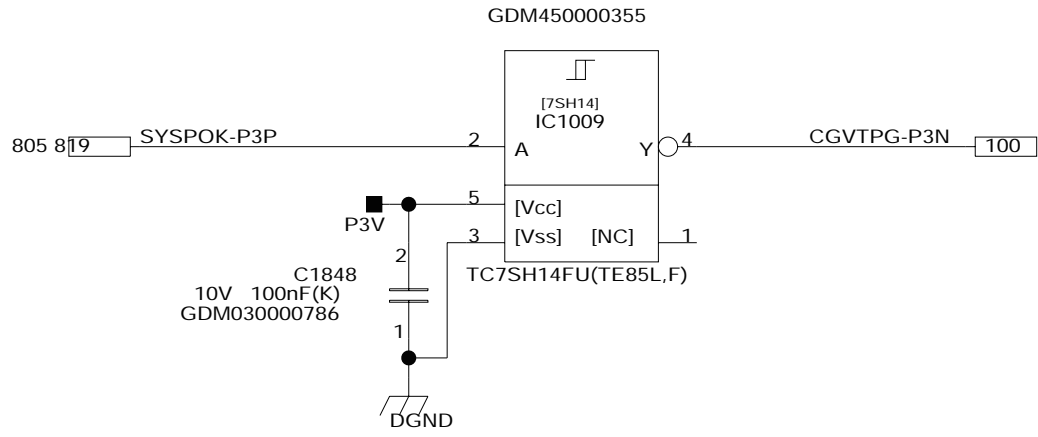
E

SCHEMATIC DIAGRAM-27 TIMING CONTROL

1



2

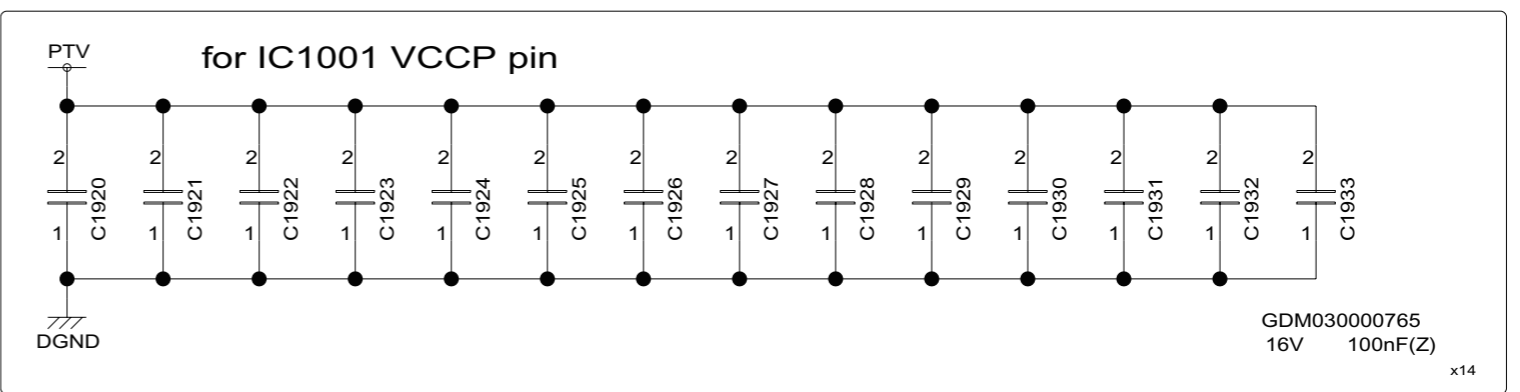
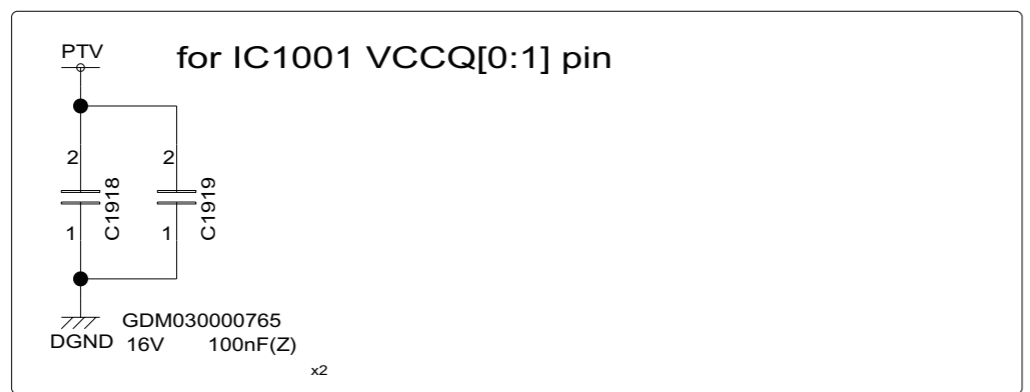
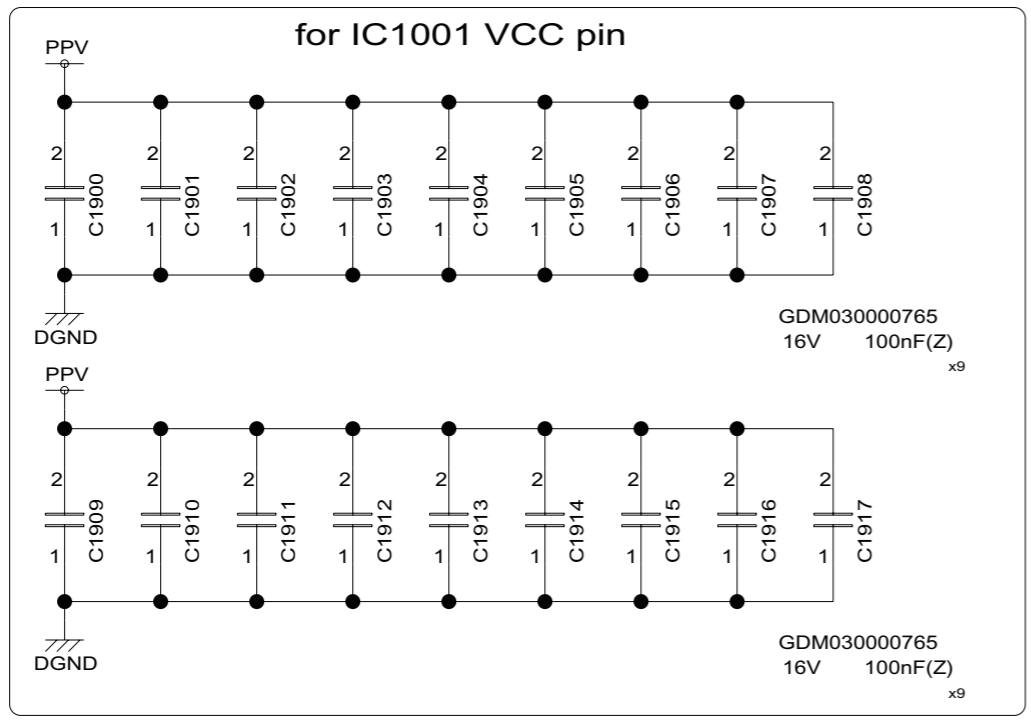


3

4

A B C D E F G H
SCHEMATIC DIAGRAM-28
ADDITIONAL CAPACITOR-3

1
2
3
4
5



A

B

C

D

E

SCHEMATIC DIAGRAM-29

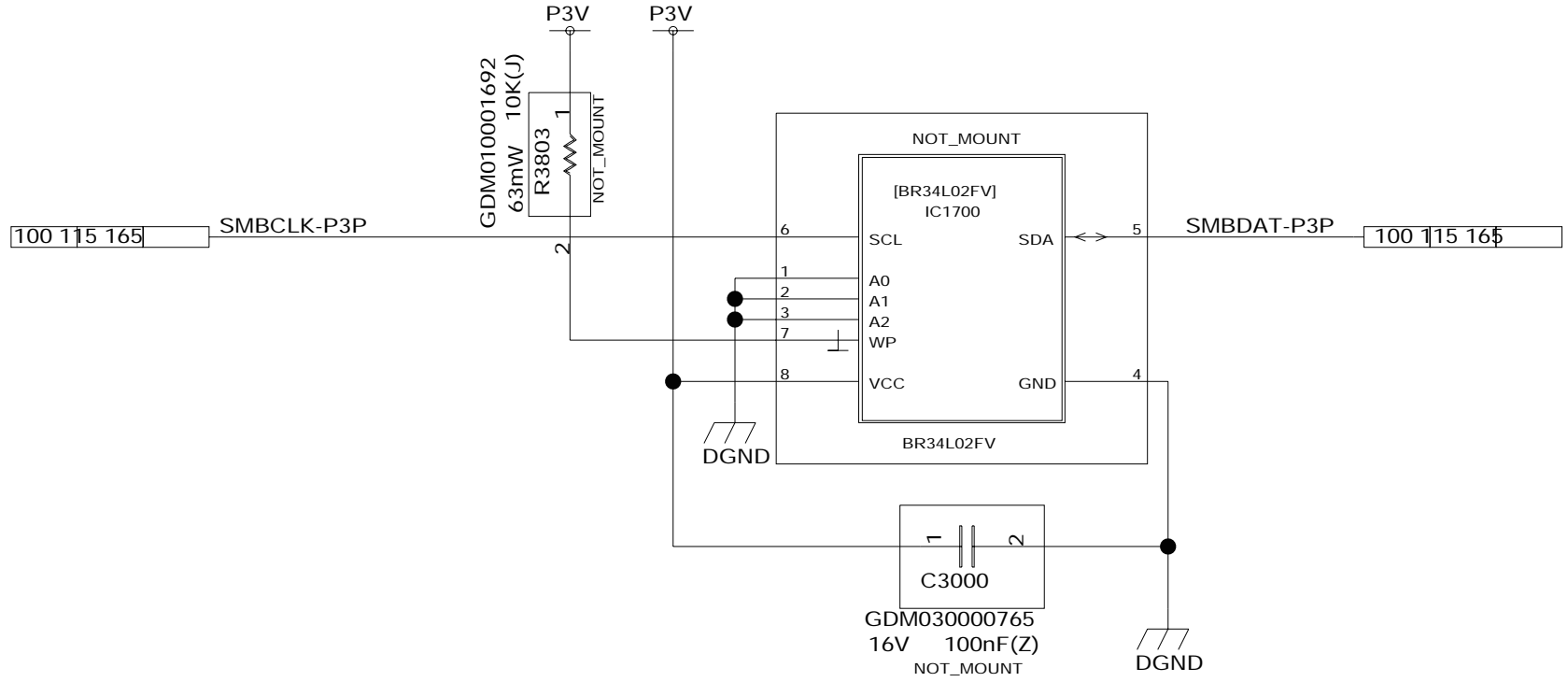
SPD SECTION

1

2

3

4



A

B

C

D

E

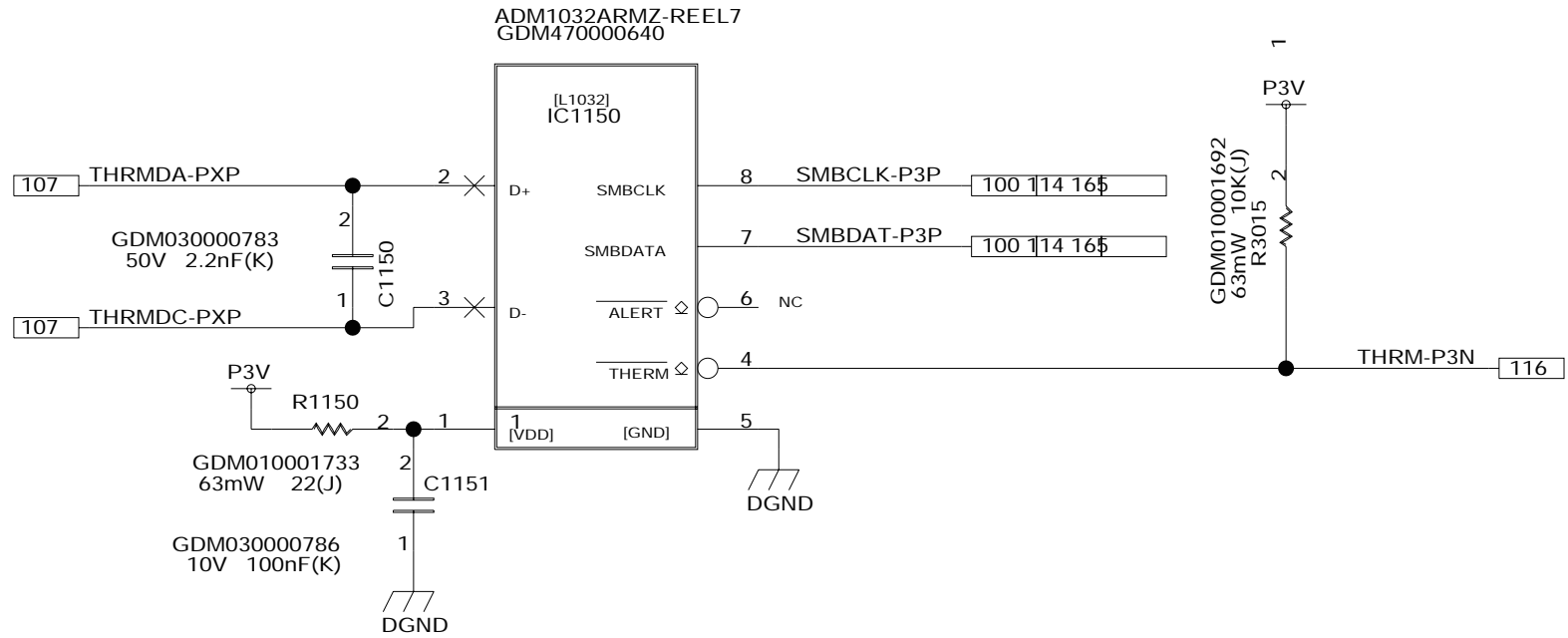
SCHEMATIC DIAGRAM-30 THERMAL SENSOR SECTION

1

2

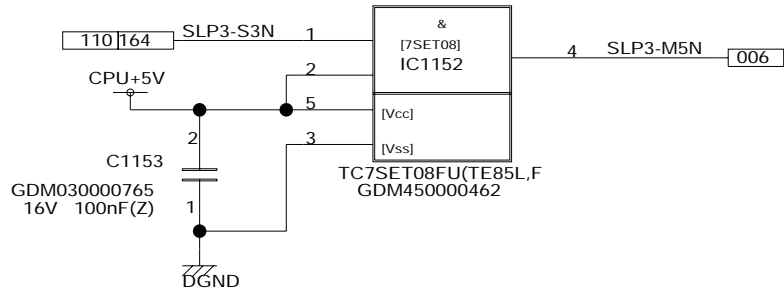
3

4

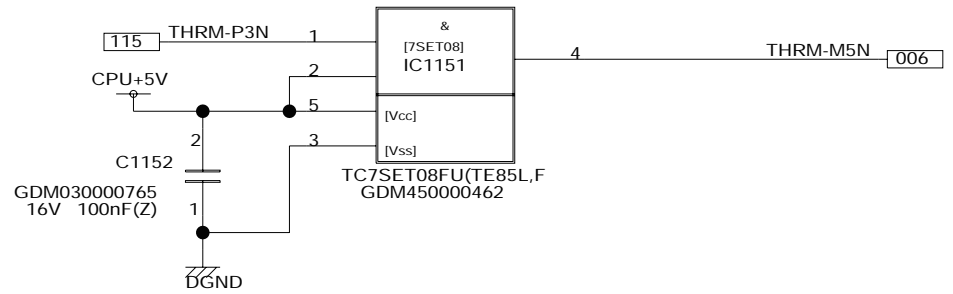


SCHEMATIC DIAGRAM-31 LEVEL SHIFT SECTION

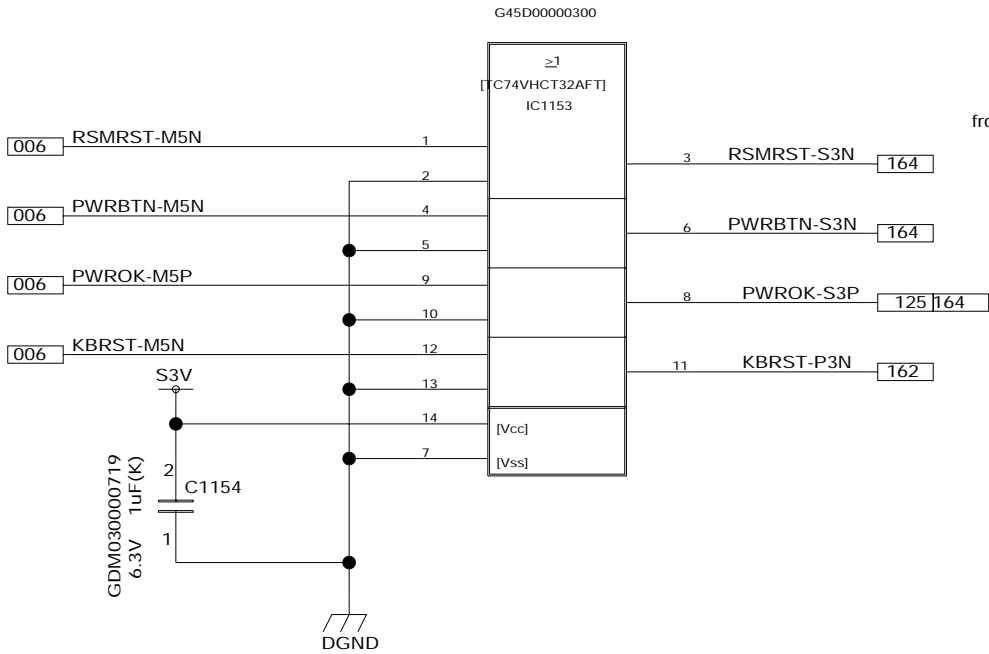
1



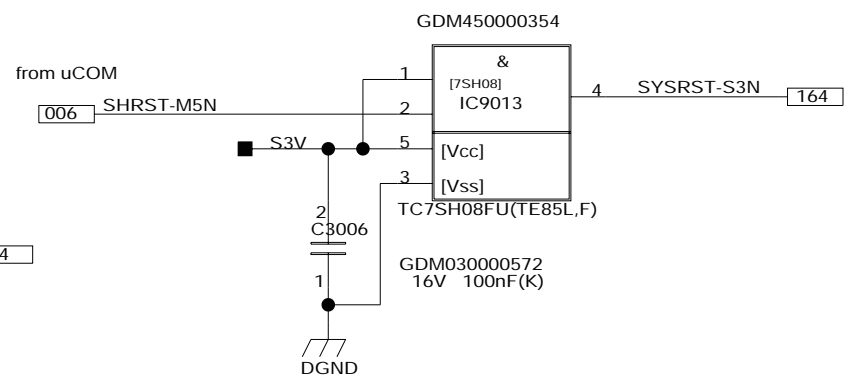
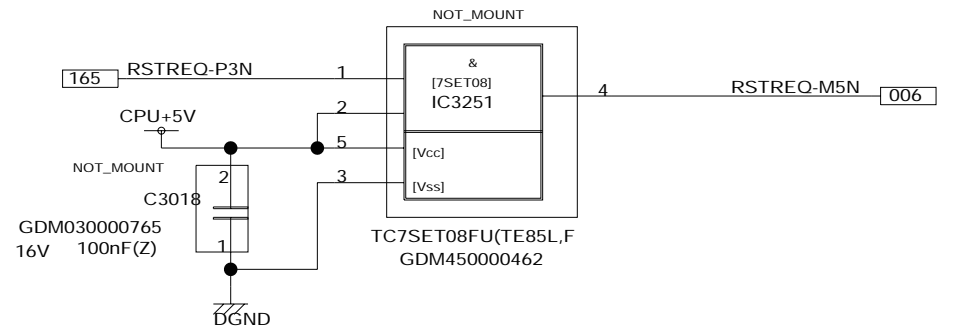
2



3



4



A

B

C

D

E

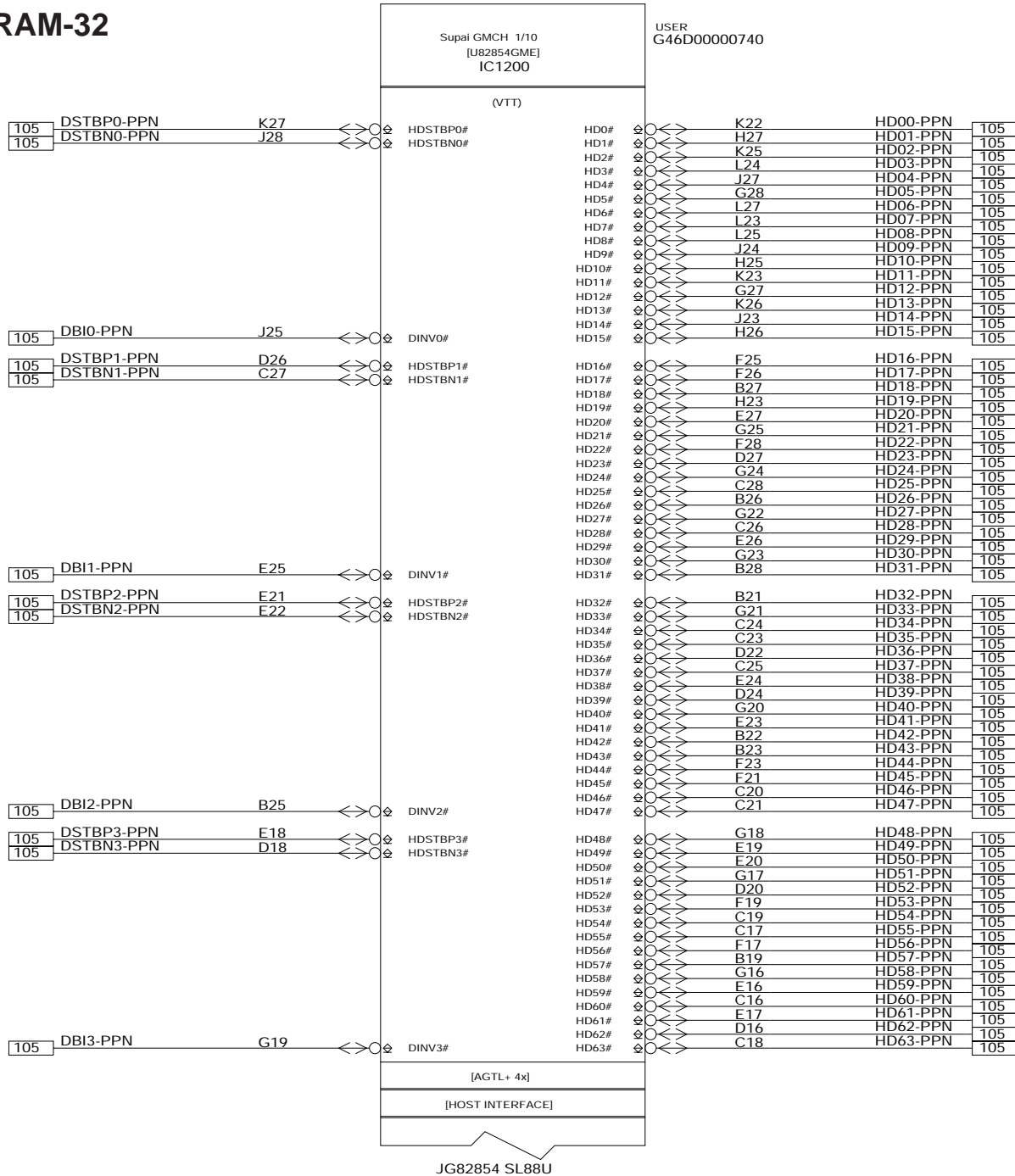
SCHEMATIC DIAGRAM-32
SUPAI_1 SECTION

1

2

3

4



A

B

C

D

E

SCHEMATIC DIAGRAM-33
SUPAI SECTION-2

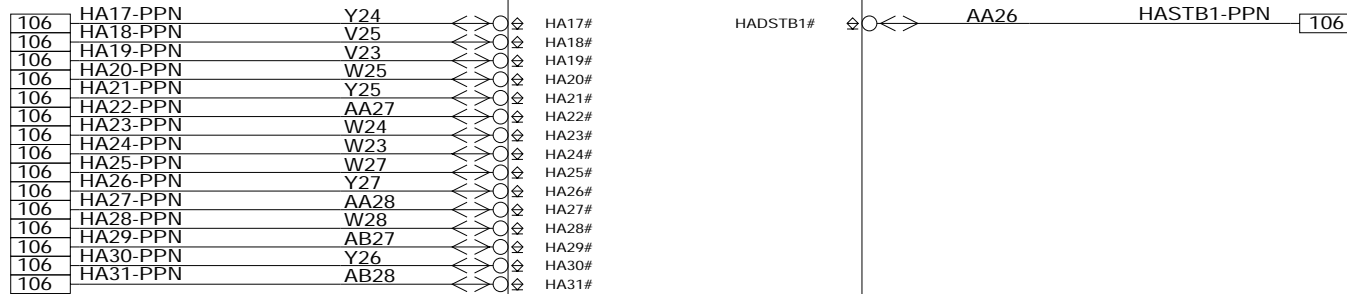
G46D00000740

Supai GMCH 2/10
[U82854GM]
IC1200

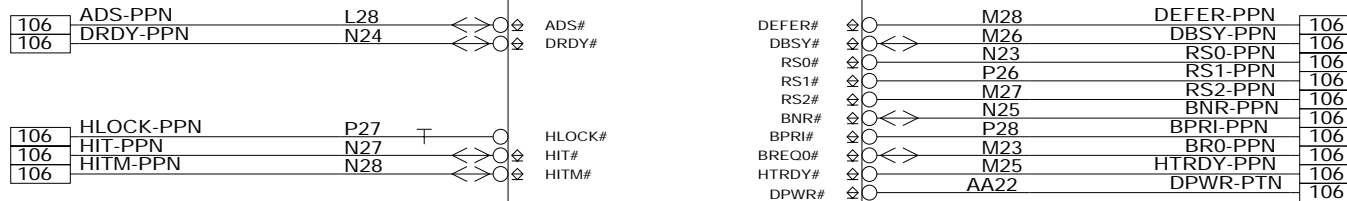
(VTT)



2



3



[AGTL+ 2x]

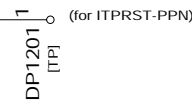
(VTT)

CPURST#



[AGTL+]

(VTT)



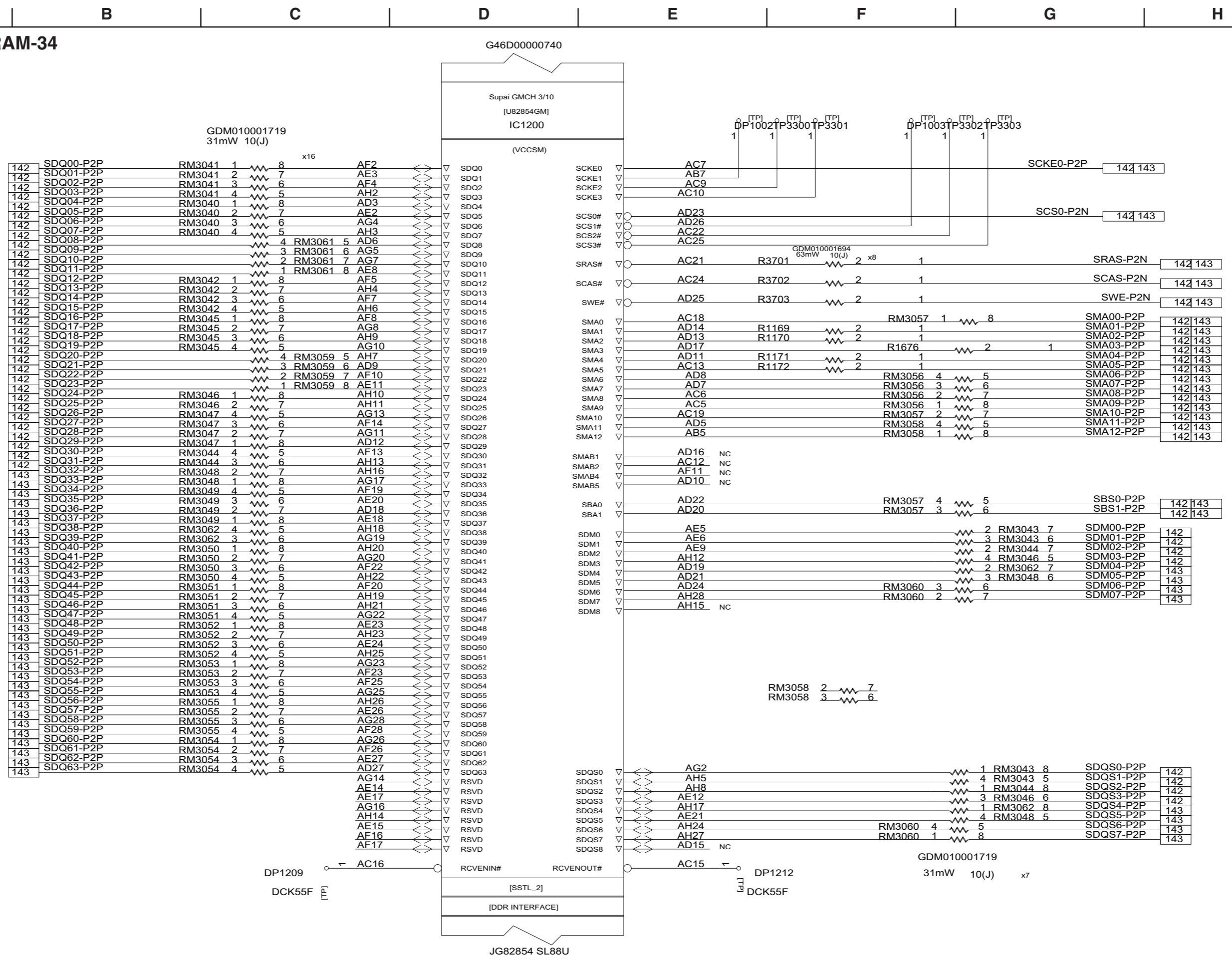
[HOST INTERFACE]

4

JG82854 SL88U

SCHEMATIC DIAGRAM-34
SUPAI SECTION-3

1
2
3
4
5



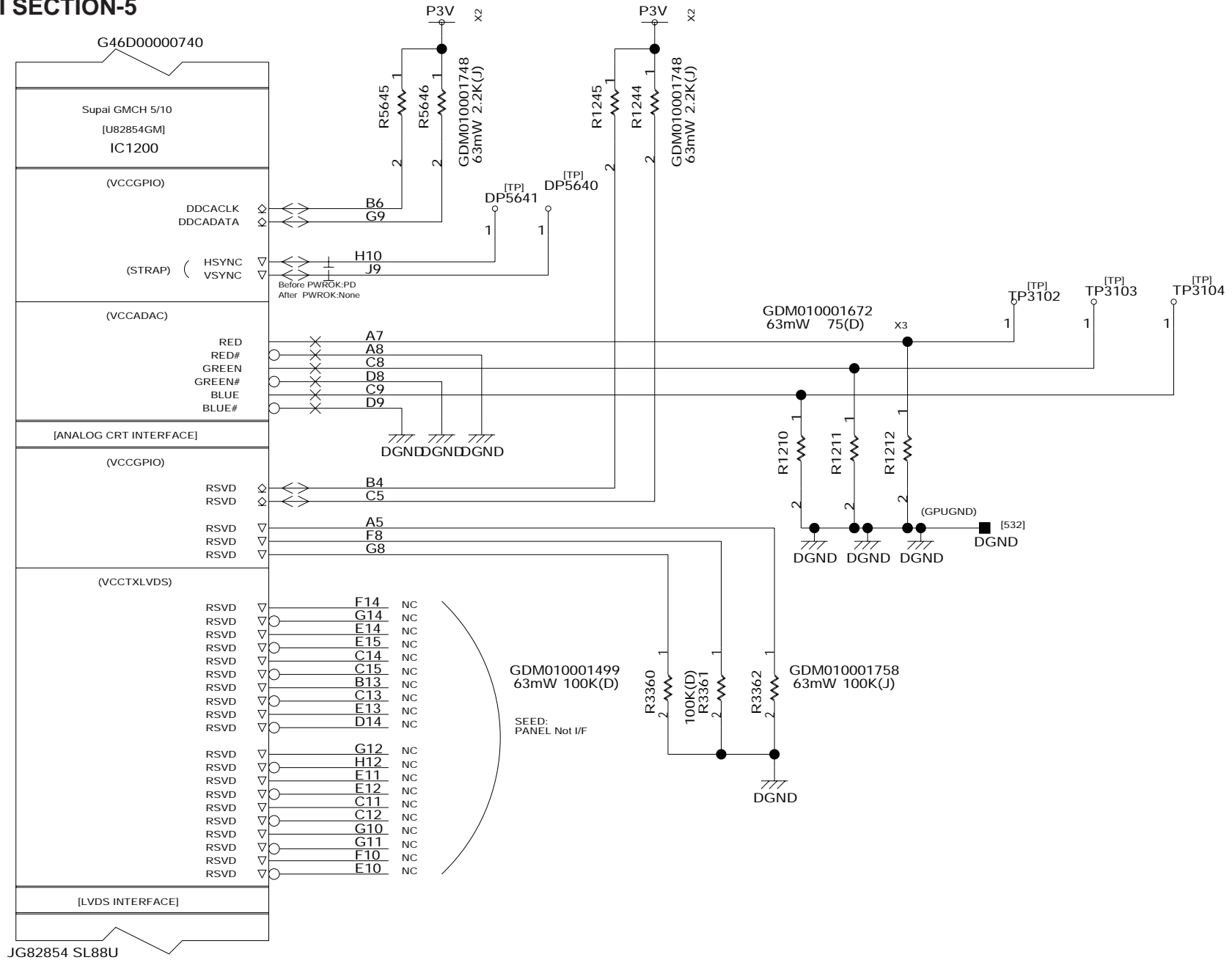
SCHEMATIC DIAGRAM-36
SUPAI SECTION-5

1

2

3

4



SCHEMATIC DUAGRAM-38
SUPAI SECTION-7

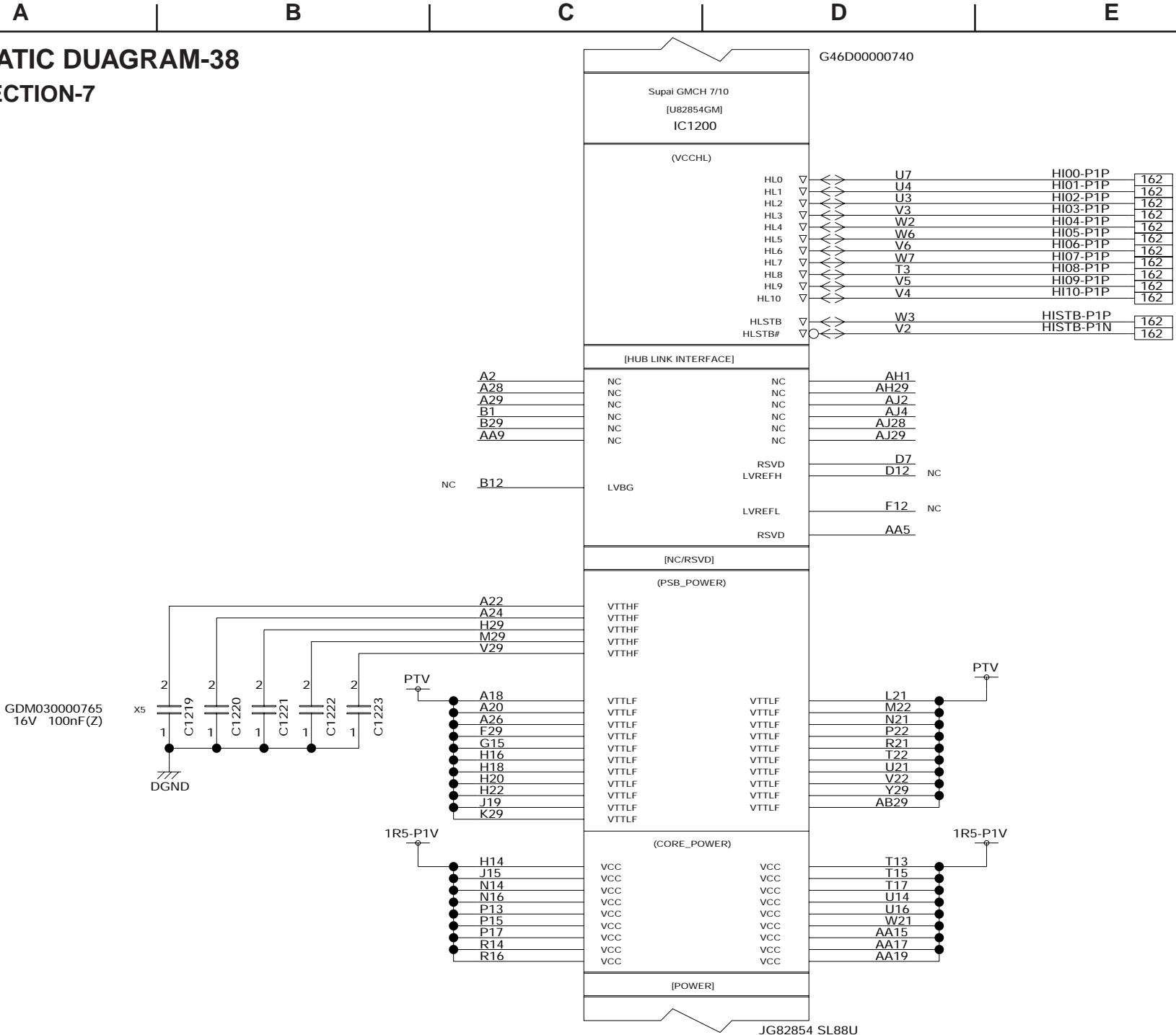
1

2

3

4

GDM030000765
16V 100nF(Z)



JG82854 SL88U

SCHEMATIC DUAGRAM-39 SUPAI SECTION-8

1

2

3

4

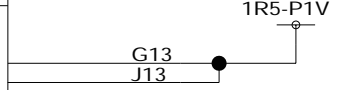
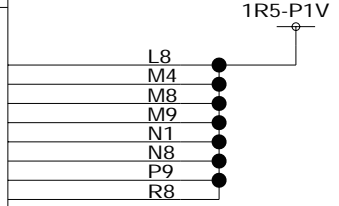
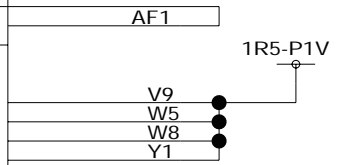
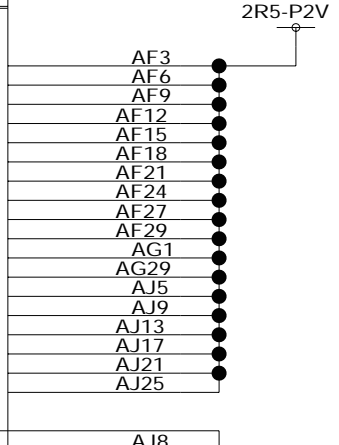
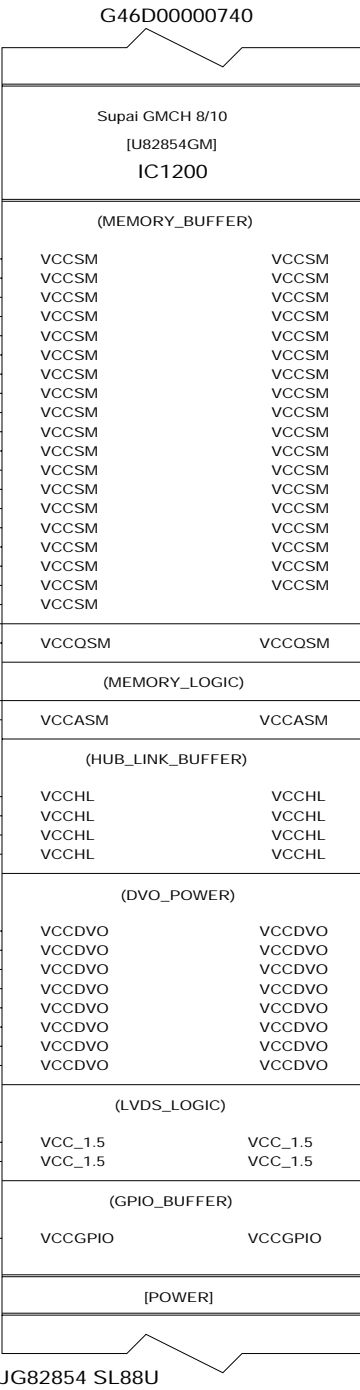
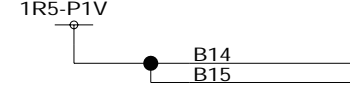
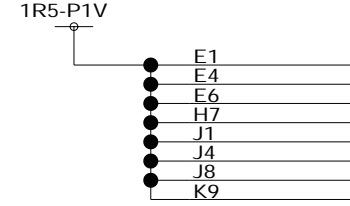
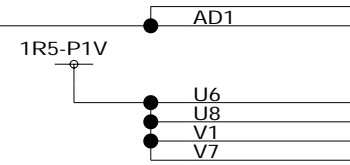
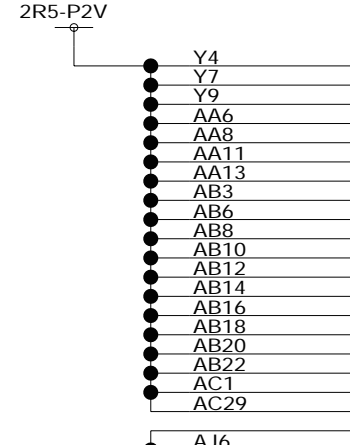
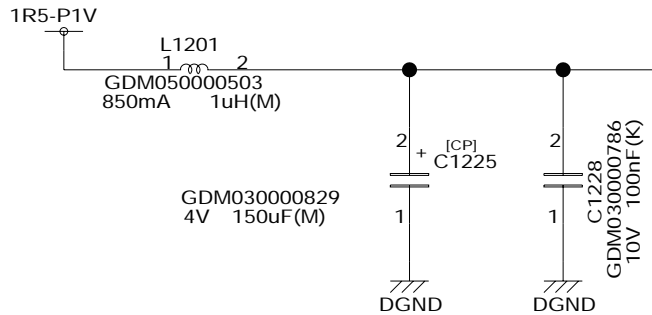
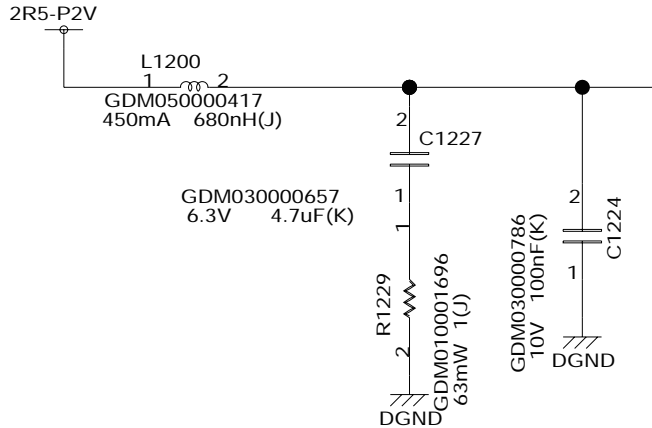
A

B

C

D

E



JG82854 SL88U

SCHEMATIC DIAGRAM-40 SUPAI SECTION-9

Note1: Route VSSADAC and VSSALVDS trace to the cap.
(No via BTW GMCH and cap)

Note2: These capacitors should be placed as close to the GMCH as possible

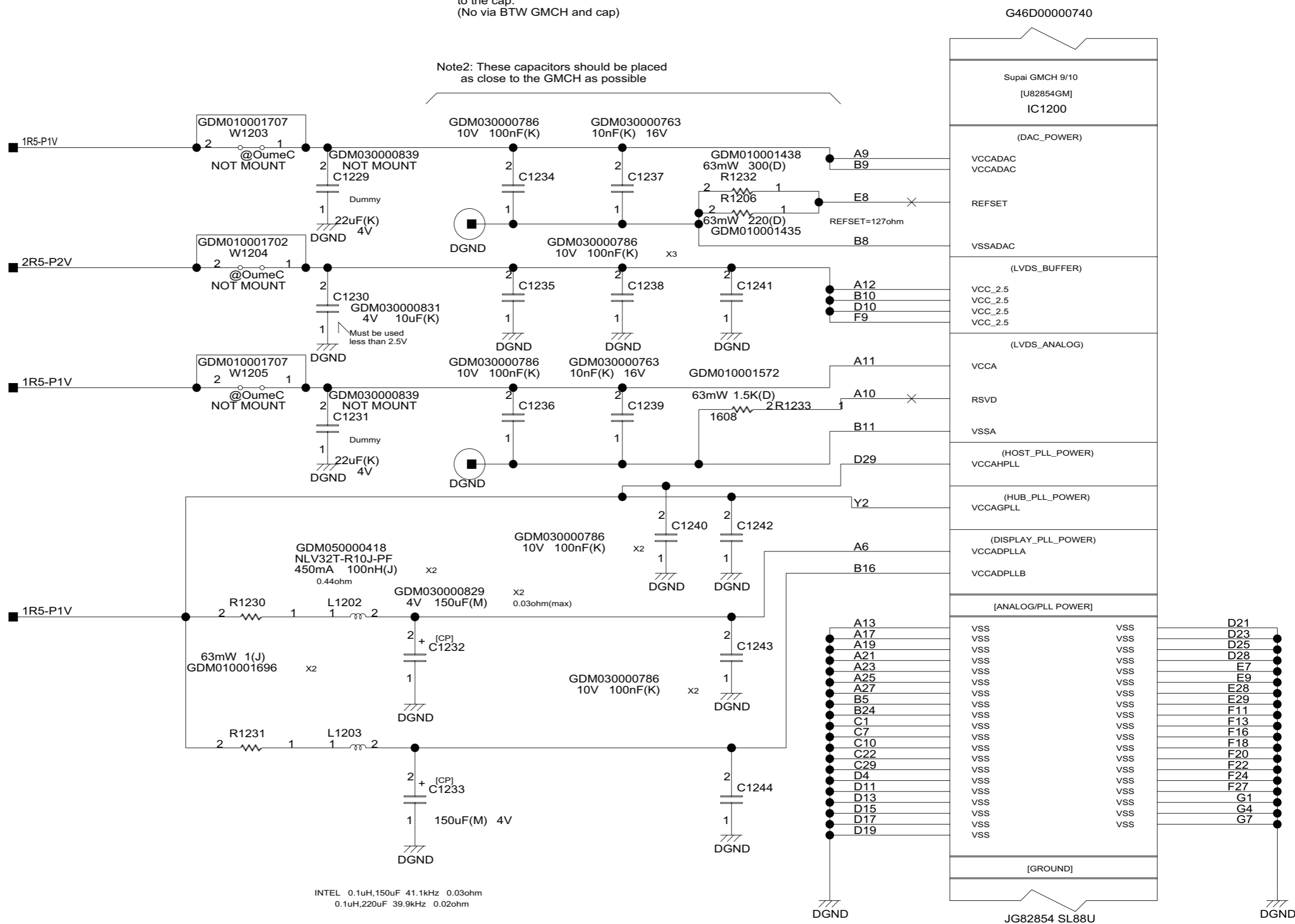
1

2

3

4

5



INTEL 0.1uH,150uF 41.1kHz 0.03ohm
0.1uH,220uF 39.9kHz 0.02ohm

A

B

C

D

SCHEMATIC DIAGRAM-41

SUPAI SECTION-10

1

G46D00000740

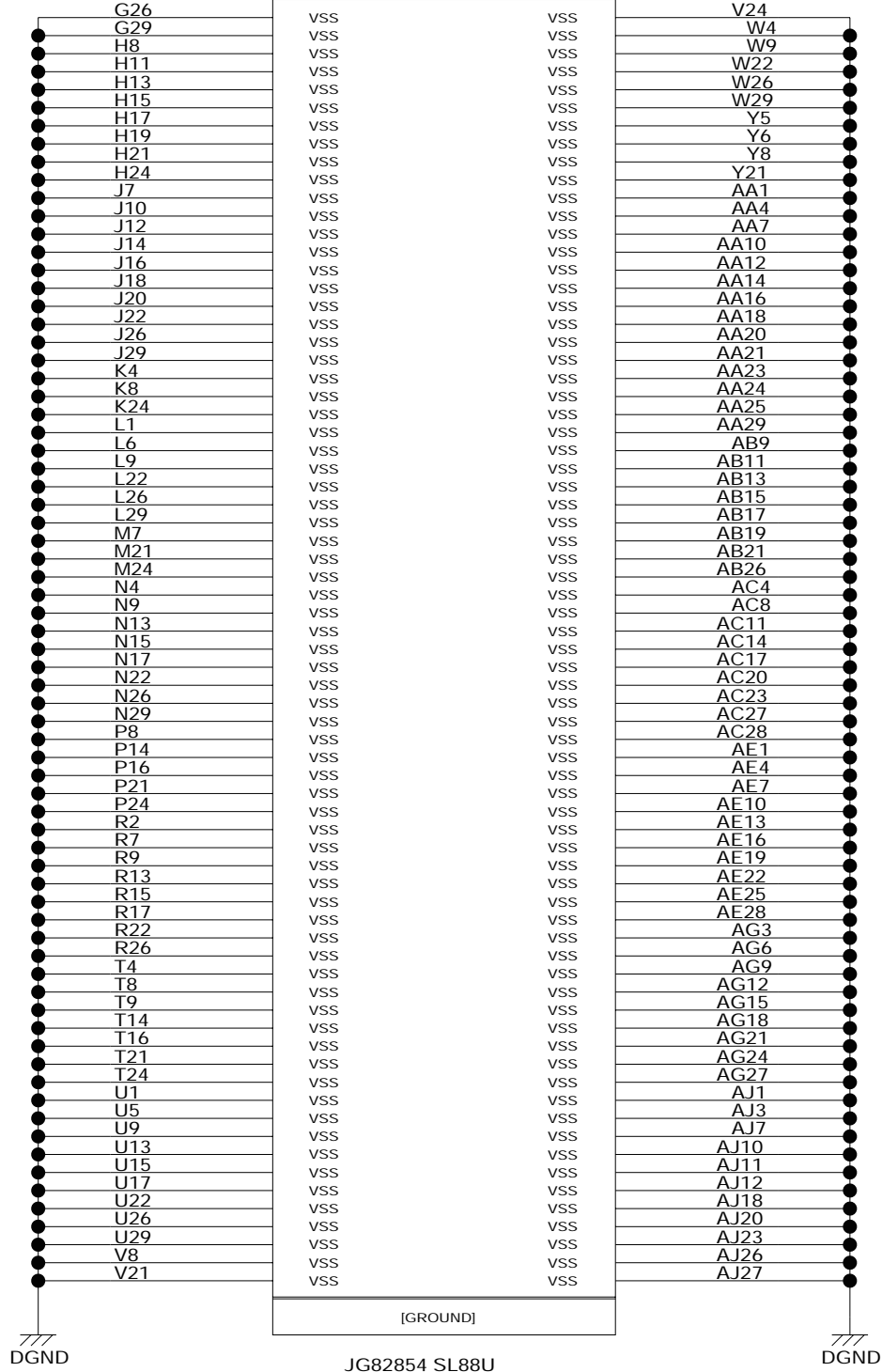
Supai GMCH 10/10
[U82854GM]
IC1200

2

3

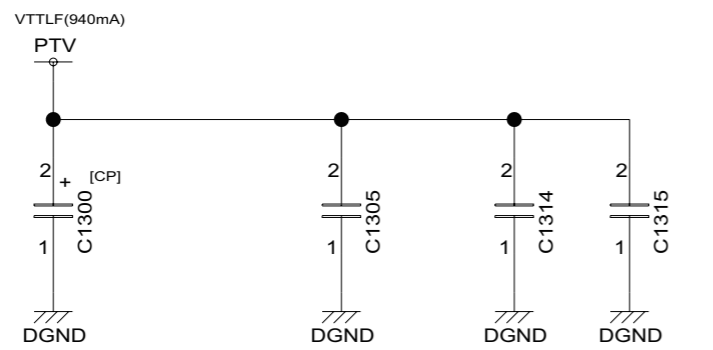
4

5



SCHEMATIC DIAGRAM-47 SUPAI SECTION-11

1



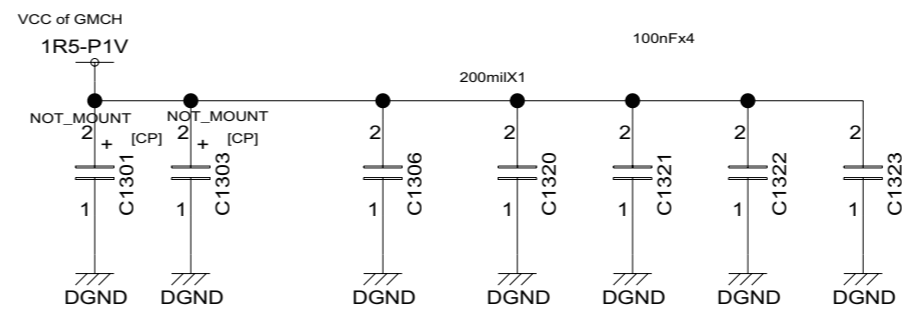
GDM030000829
4V 150uF(M)

GDM030000765
16V 100nF(Z)

GDM030000831
4V 10uF(K)

GDM030000765
16V 100nF(Z)

2



NOT MOUNT
GDM030000829 x2
4V 150uF(M)

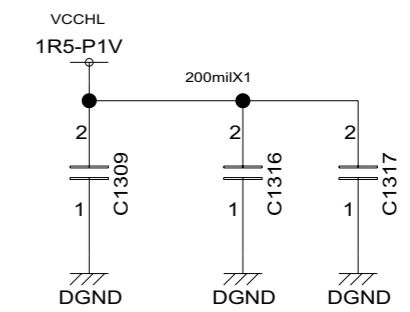
GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)

GDM030000831
4V 10uF(K)

GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)

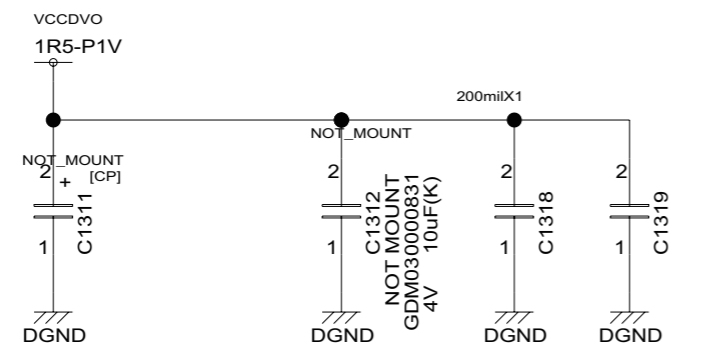


GDM030000765
16V 100nF(Z)

GDM030000831
4V 10uF(K)

GDM030000765
16V 100nF(Z)

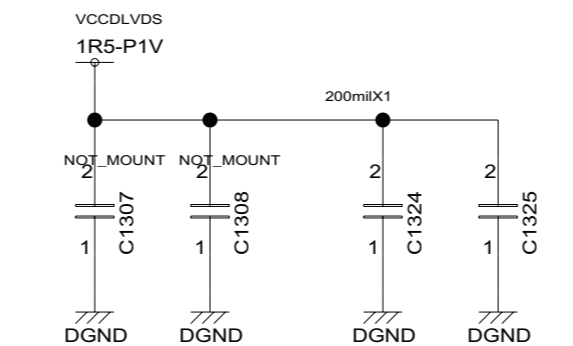
3



NOT MOUNT
GDM030000829
4V 150uF(M)

GDM030000765
16V 100nF(Z)

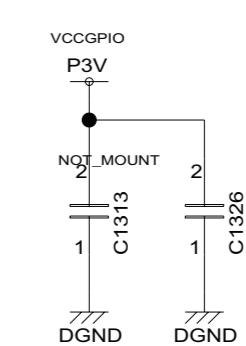
GDM030000765
16V 100nF(Z)



GDM030000758 x2
6.3V 22uF(K)

GDM030000765
16V 100nF(Z)

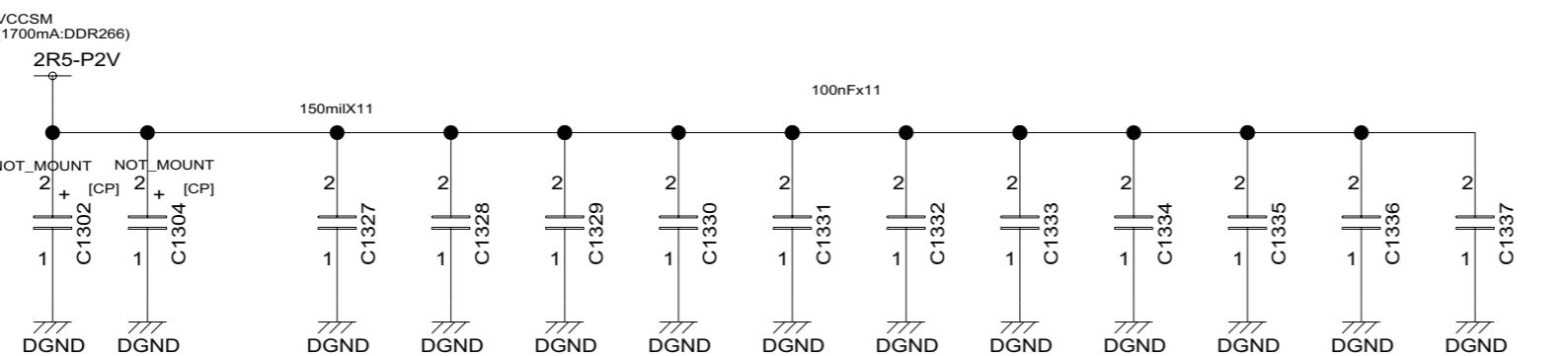
GDM030000765
16V 100nF(Z)



NOT MOUNT
GDM030000748
6.3V 10uF(K)

GDM030000765
16V 100nF(Z)

4



NOT MOUNT
GDM030000829 x2
4V 150uF(M)

GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)

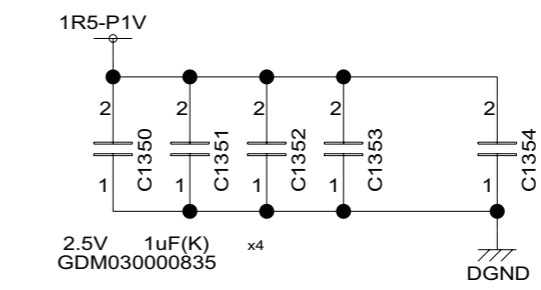
GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)

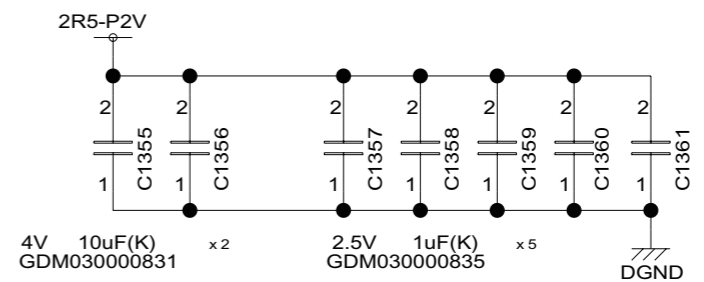


2.5V 1uF(K) x4
GDM030000835

Lumos:1PH8-CR-03A042
1.5V
4V 10uF (2012) x2
2.5V 1uF (1005) x4
16V 100nF (1005) x12

2.5V
4V 10uF (2012) x2
2.5V 1uF (1005) x5
16V 100nF (1005) x5

C1301, C1312, C1302, C1328
C1331, C1333-C1336
Not Mount
C1350-C1361 ADDED



4V 10uF(K) x2
GDM030000831

2.5V 1uF(K) x5
GDM030000835

5

A

B

C

D

E

SCHEMATIC DIAGRAM-43

SUPAI SECTION (STRAP)

1

	L	H
LCLKCTRLB (def=L)	P-M Processor (1.2V Core)	P4 Processor/Mobile P4-M Processor (1.5V Core)
HSYNC (def=L)	Normal_Op.	XOR_test
VSYNC (def=L)	Normal_Op.	AIIZ_test
DVODETECT (def=L)	DVO	AGP
ADDID[0]	RGBA mode	Native Graphic mode
ADDID[7]	DVO device ○	DVO device ×
GSTJ[2:0]	during CPURST# internal pulled-down after CPURST# and C3/D1/D3 Hi-Z	

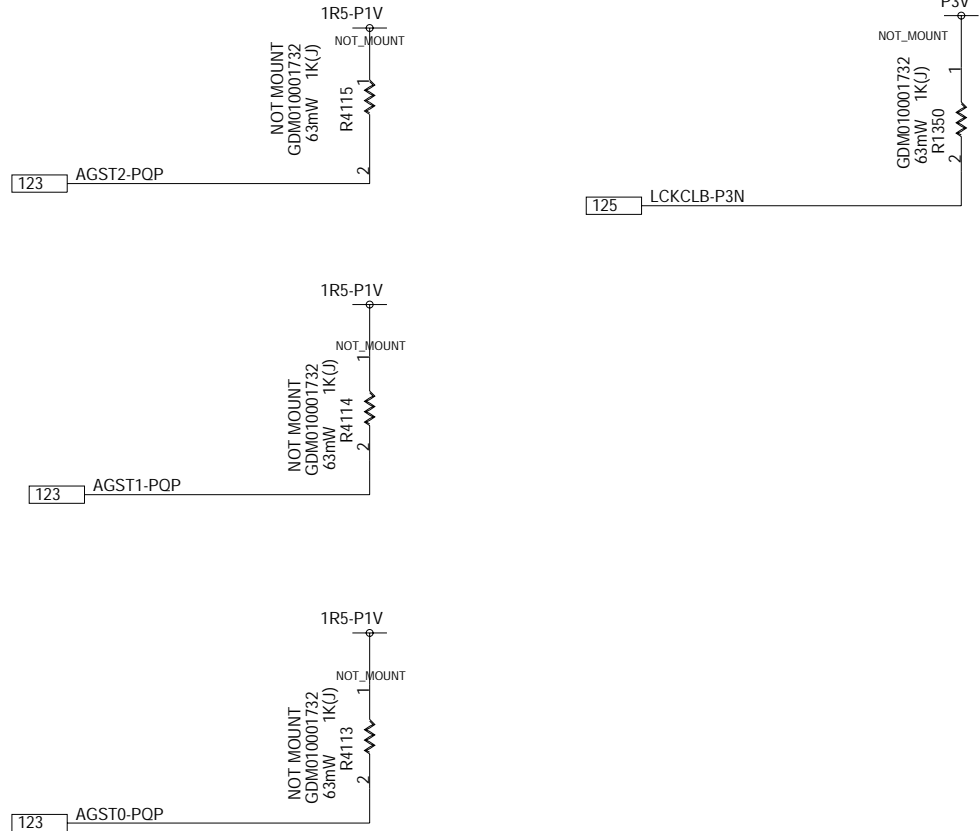
2

GSTJ[210]	PSB	MEM	GFX
000	400	266	200
001	400	200	200
100	533	266	200
101	533	266	266
110	533	333	266
111	400	333	250

3

FS[210]	CPUCLK
000	66
001	100
010	200
011	133

4

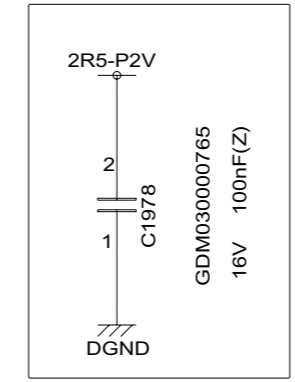
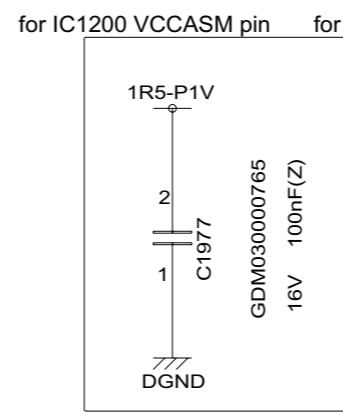
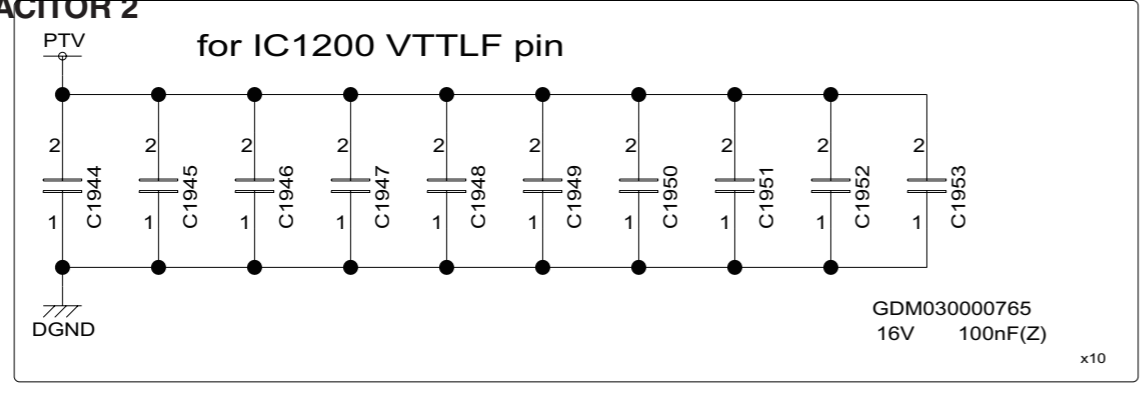


A B C D E F G H

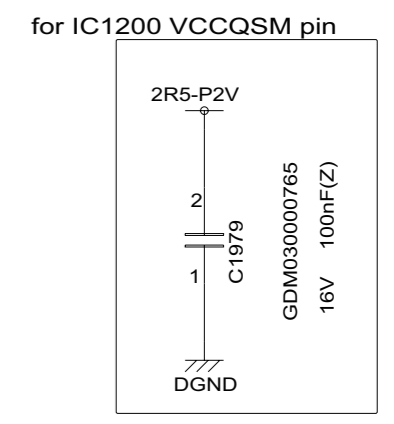
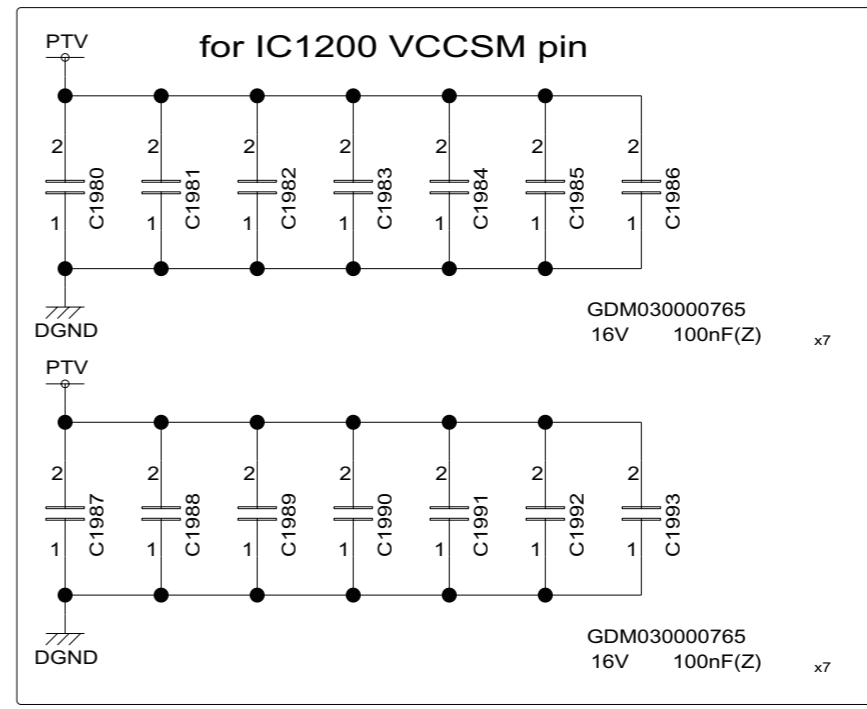
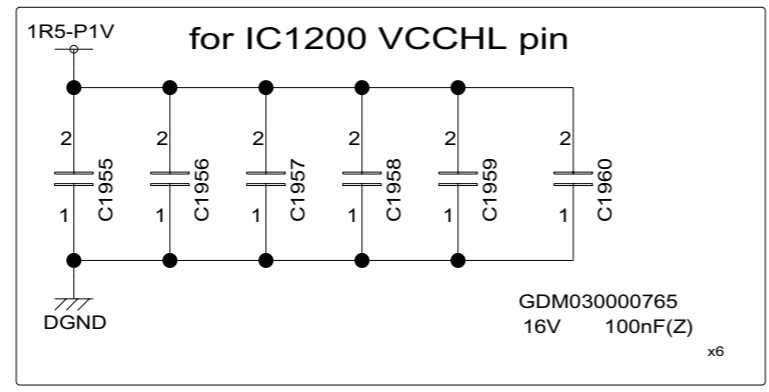
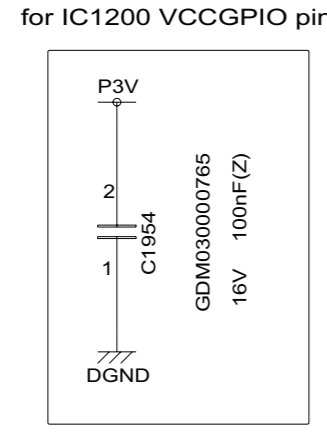
SCHEMATIC DIAGRAM-44

ADDITIONAL CAPACITOR 2

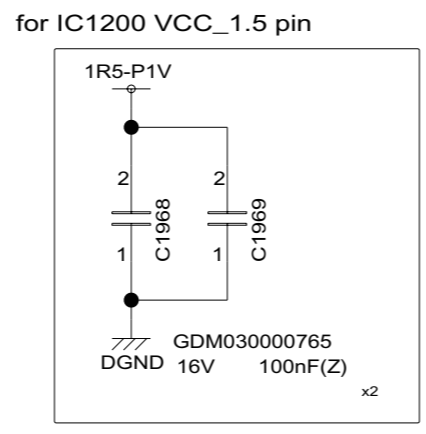
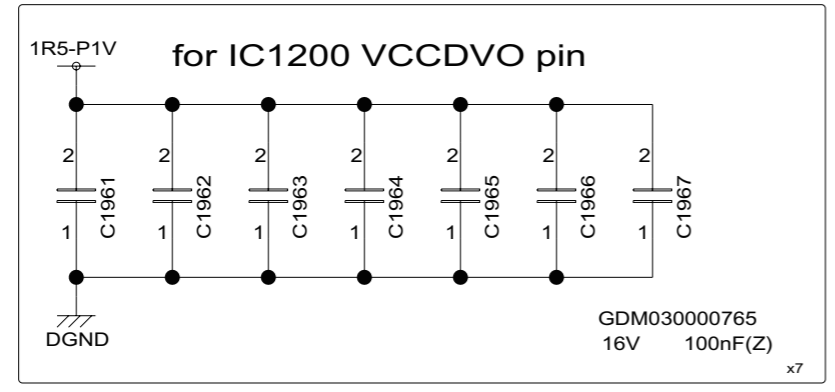
1



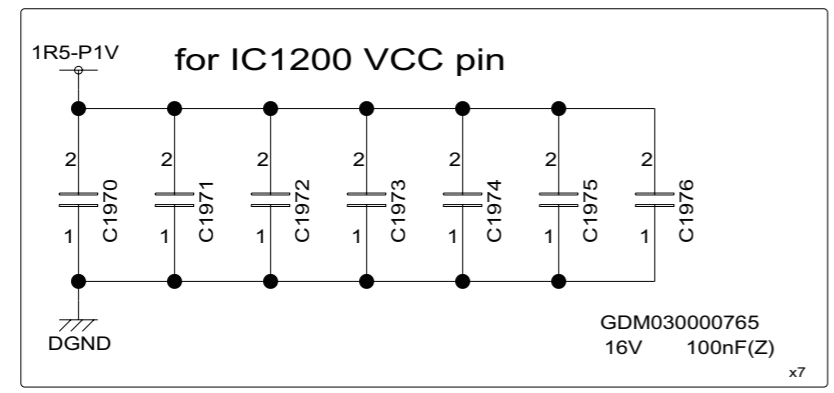
2



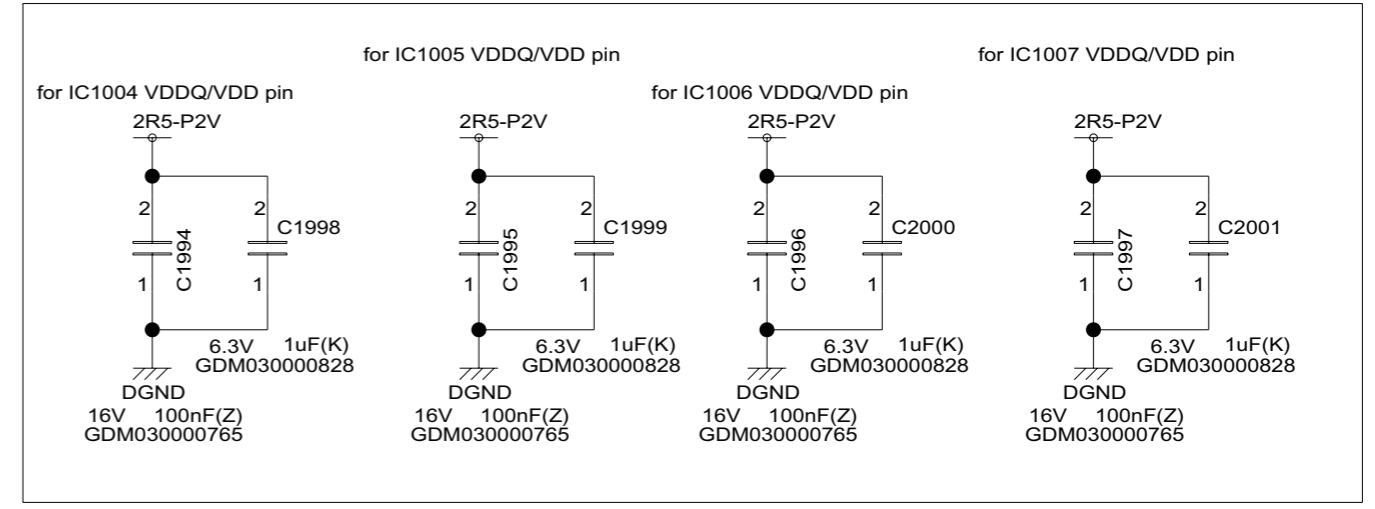
3



4



<DDR Memory(sh142,143)>



5

A B C D E F G H

SCHEMATIC DIAGRAM-45
DDR-1

GDM460001239

TSOP II
[MDS32M16]
IC1004

TSOP II
[MDS32M16]
IC1005

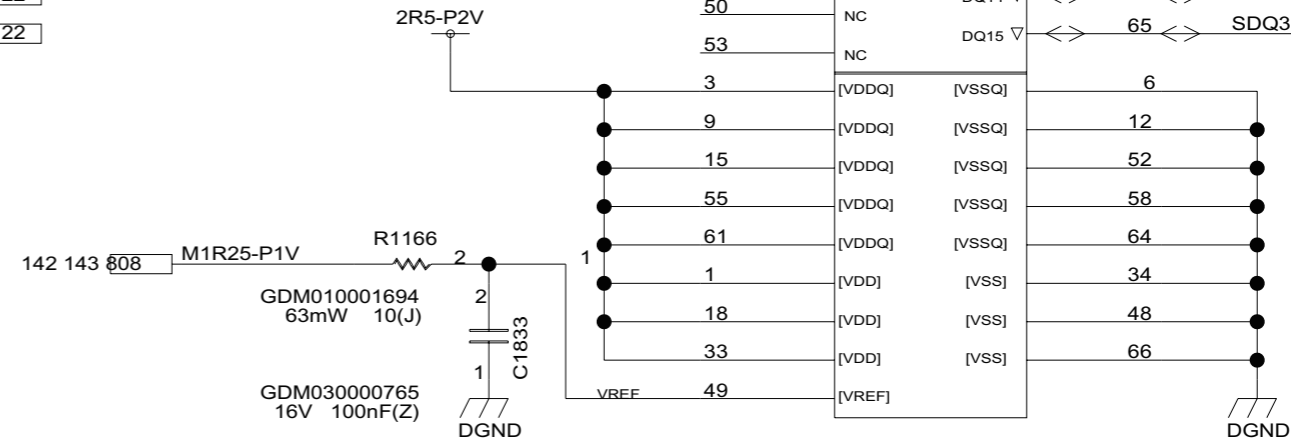
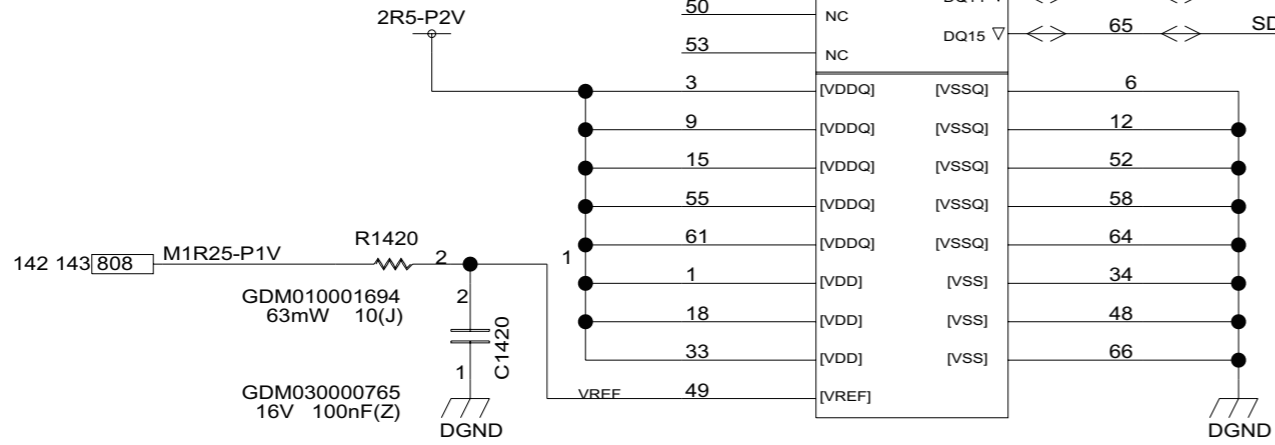
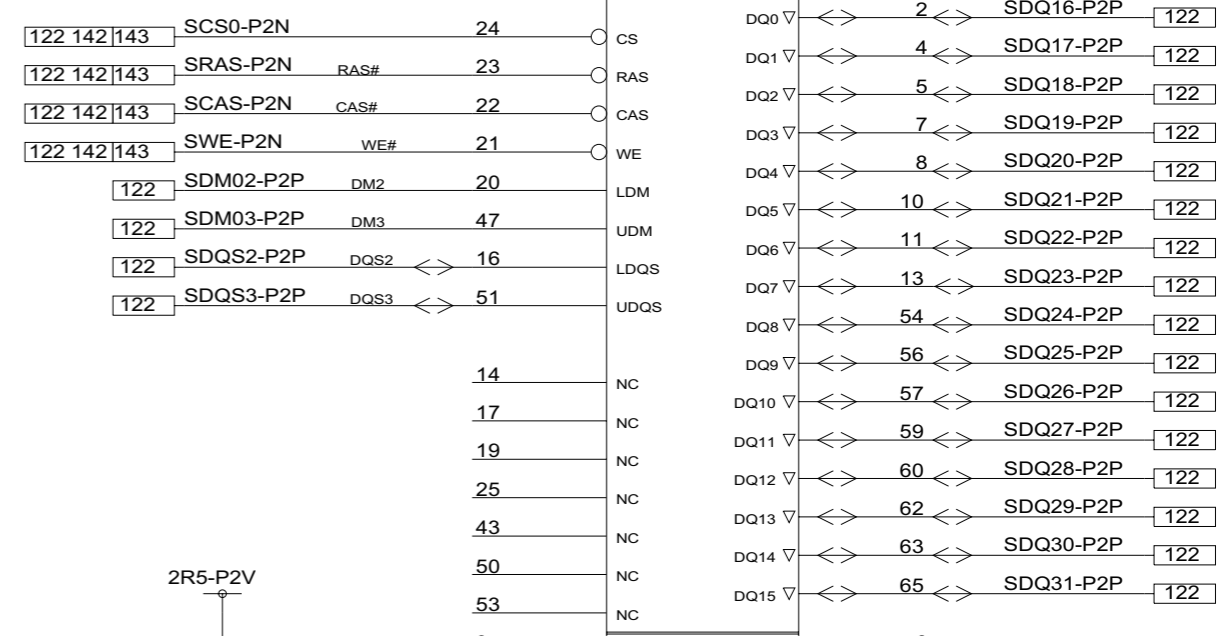
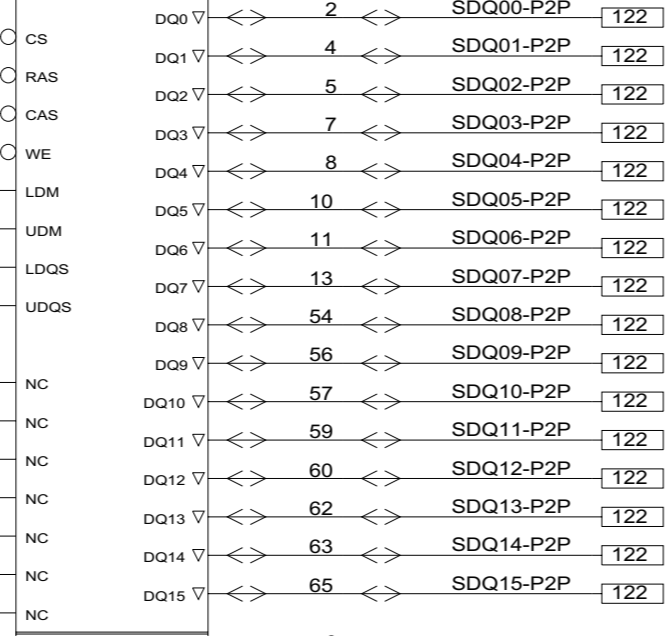
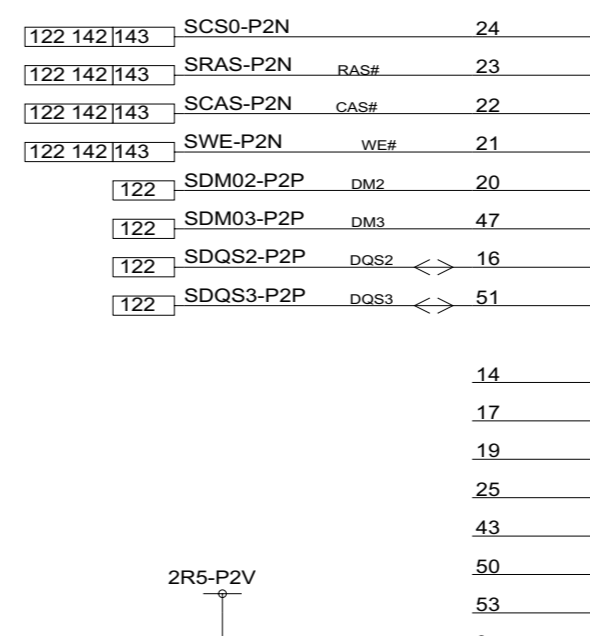
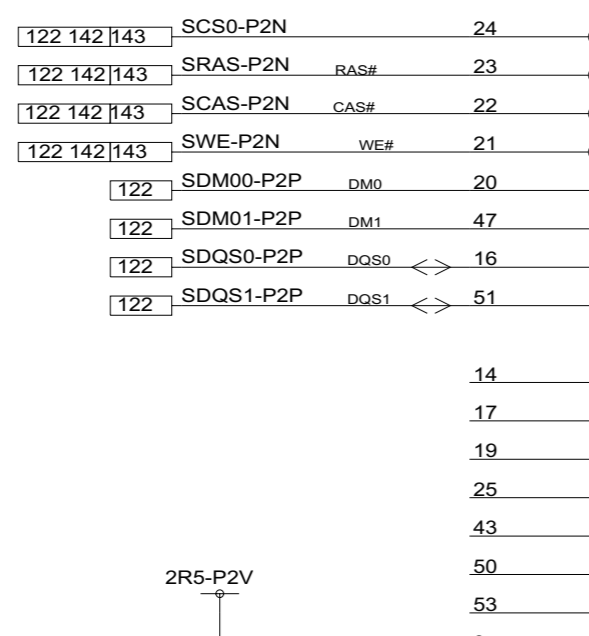
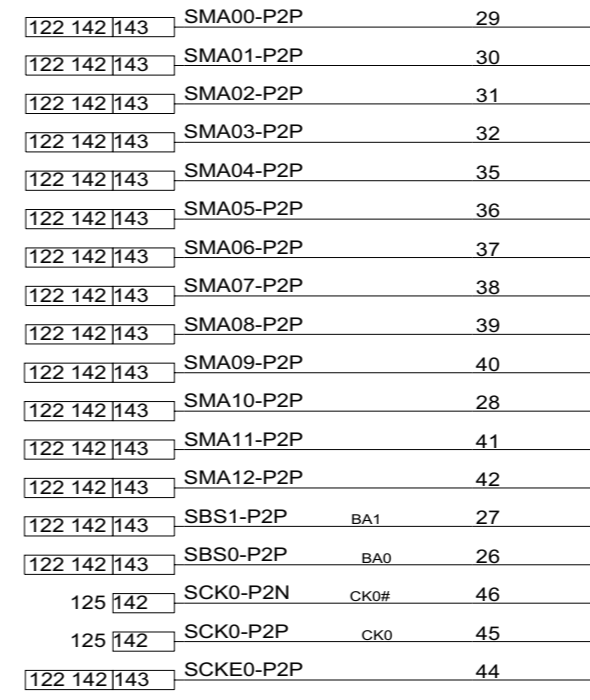
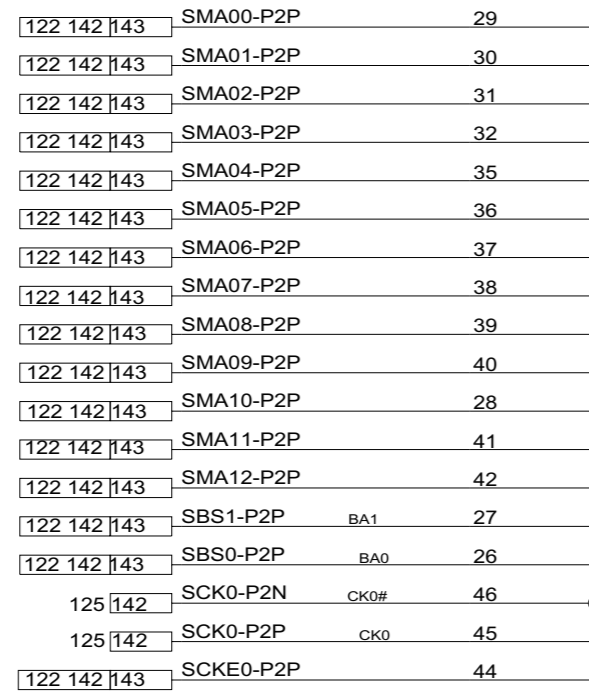
1

2

3

4

5



SCHEMATIC DIAGRAM-46

DDR-2

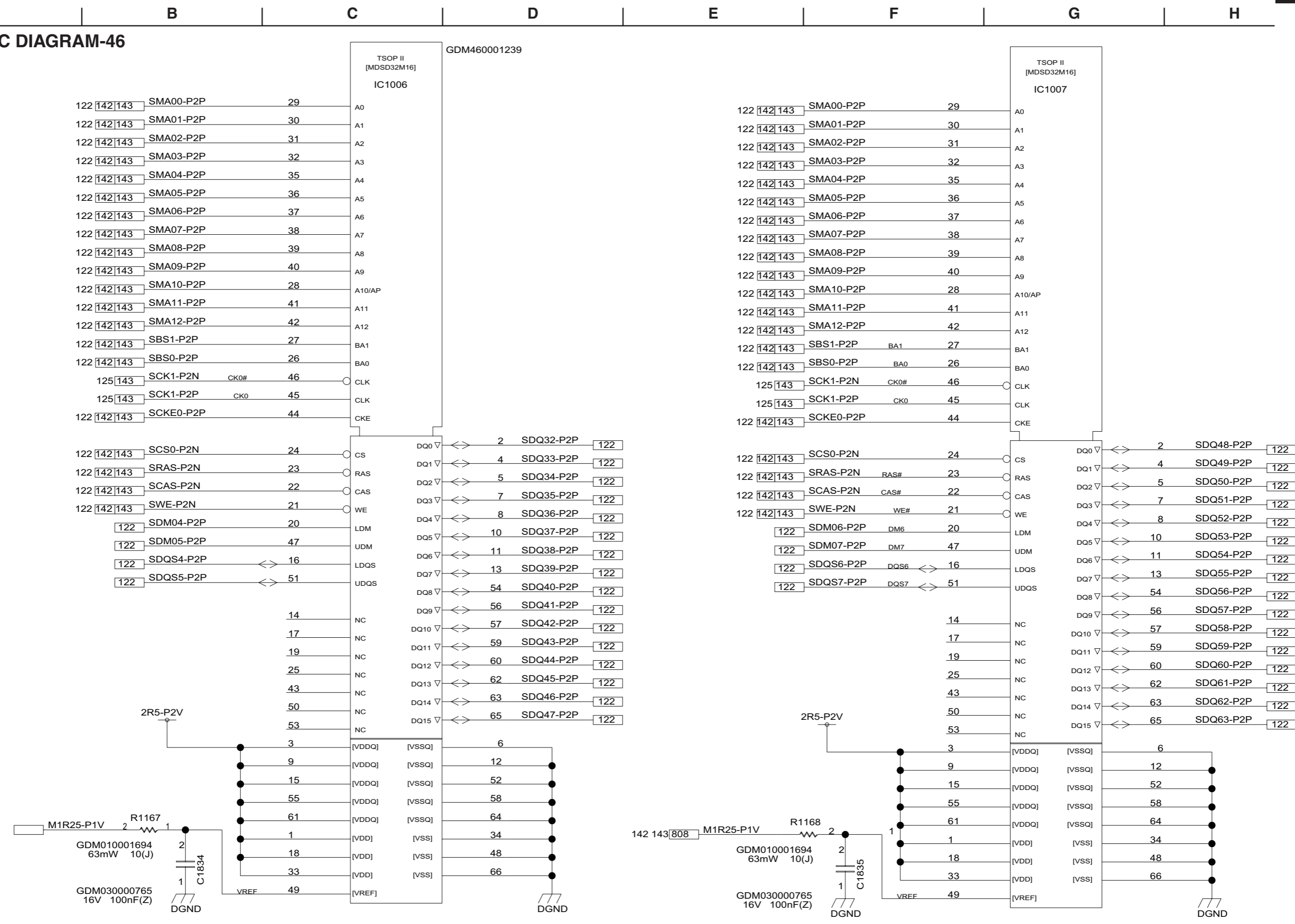
1

2

3

4

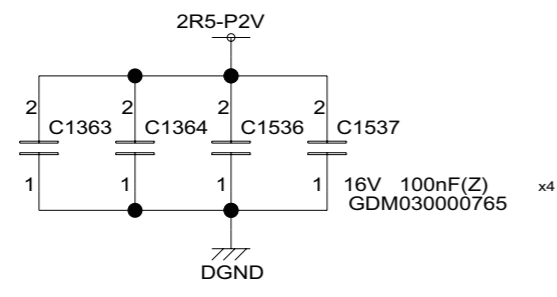
5



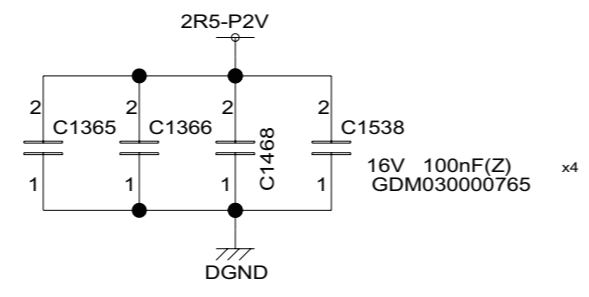
SCHEMATIC DIAGRAM-47
DDR DECOUPLING

DDR Decoupling

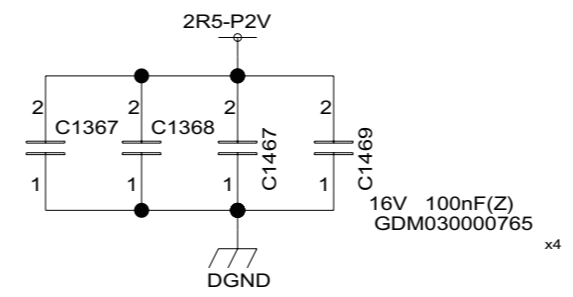
for IC1004



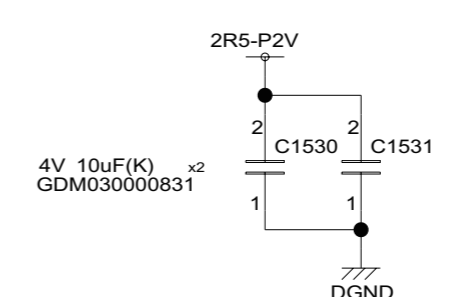
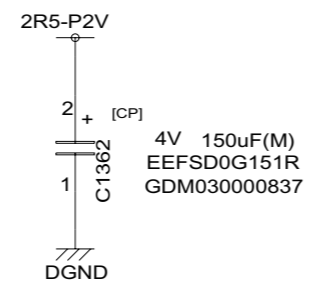
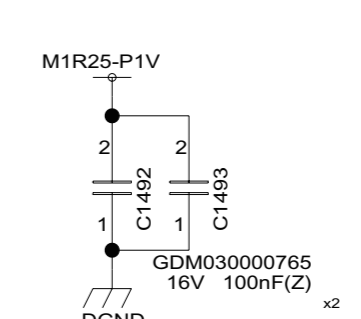
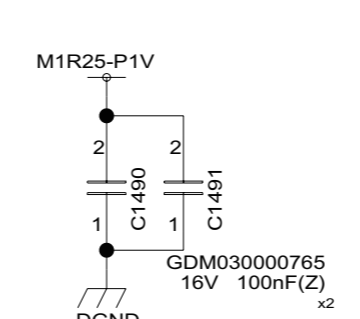
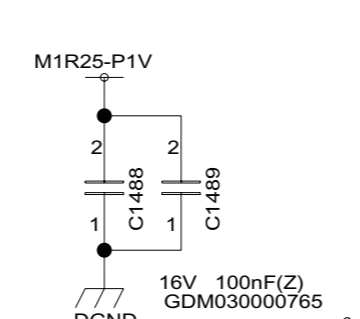
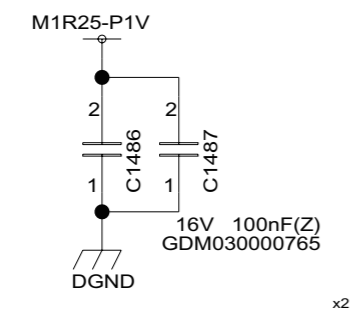
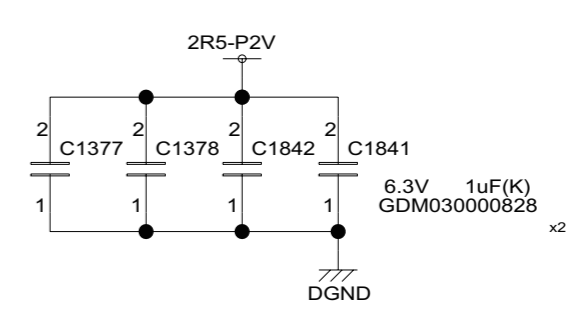
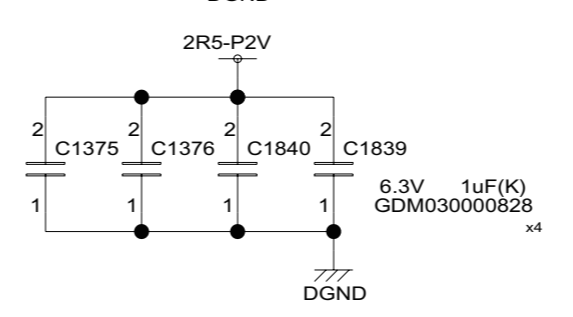
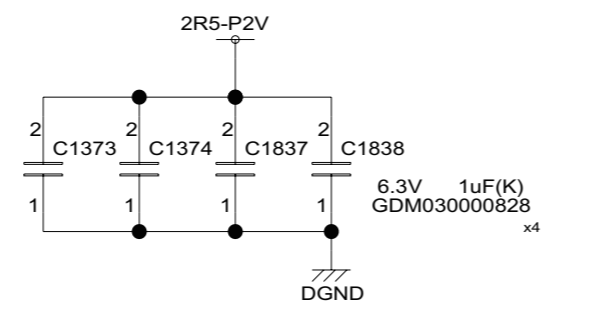
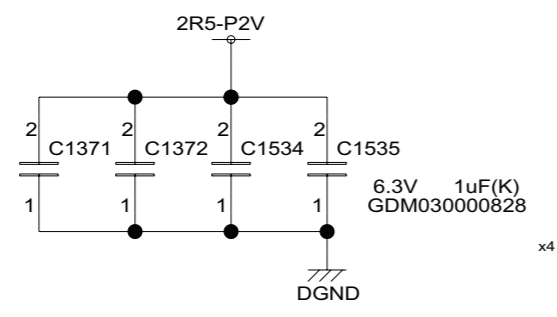
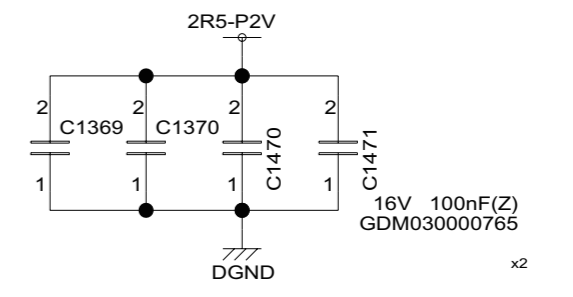
for IC1005



for IC1006

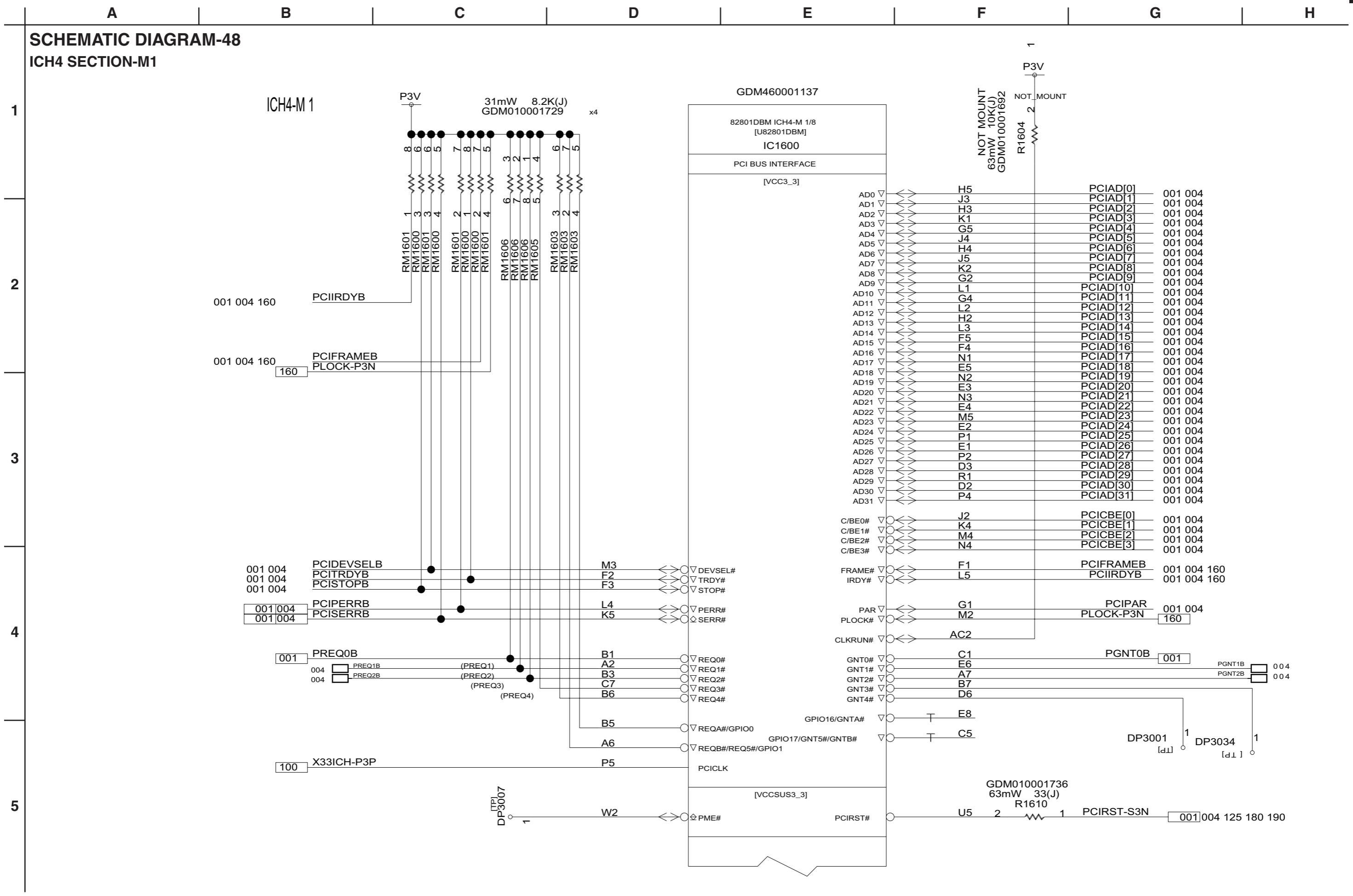


for IC1007



1
2
3
4
5

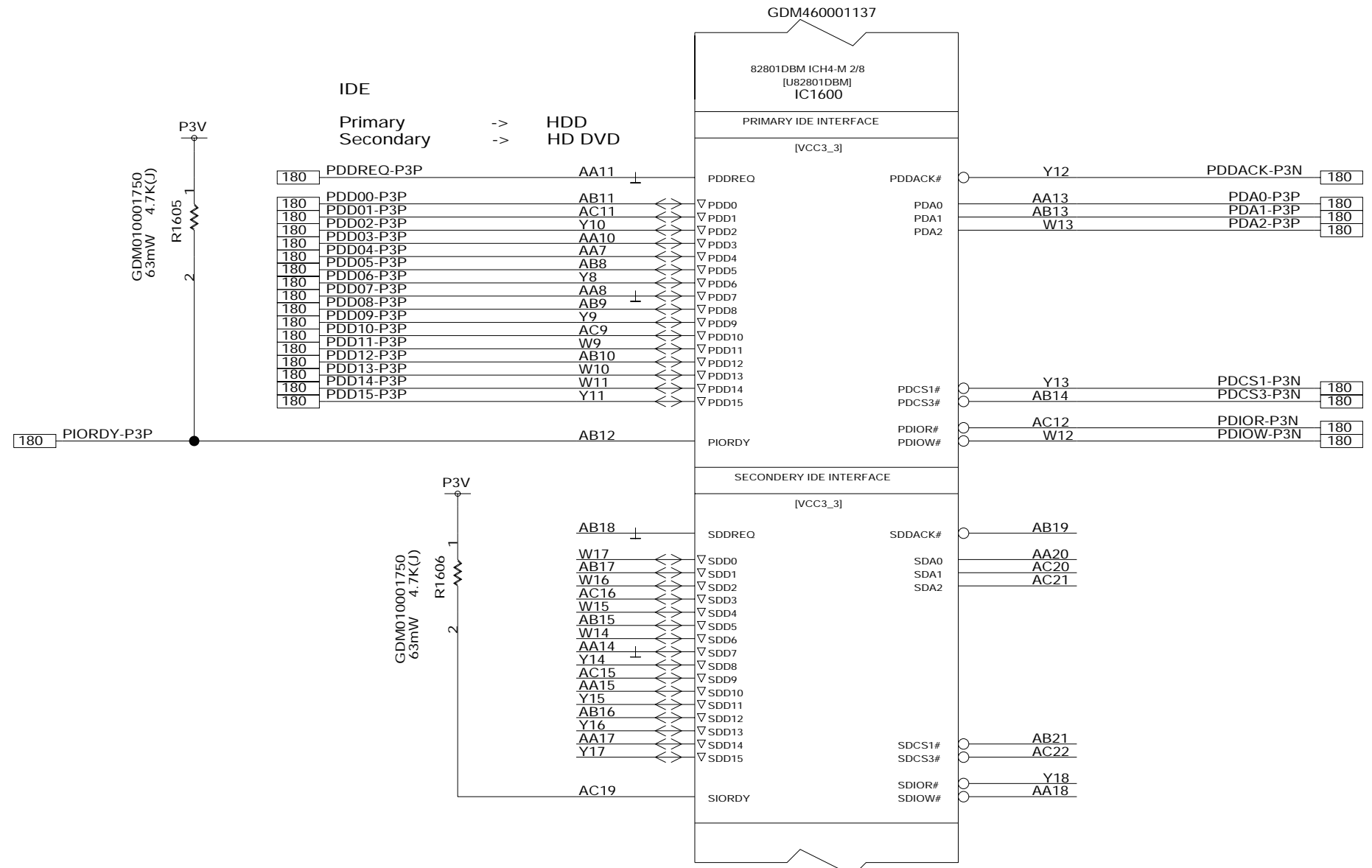
SCHEMATIC DIAGRAM-48 ICH4 SECTION-M1



SCHEMATIC DIAGRAM-49
ICH4 SECTION-M2

1
2
3
4

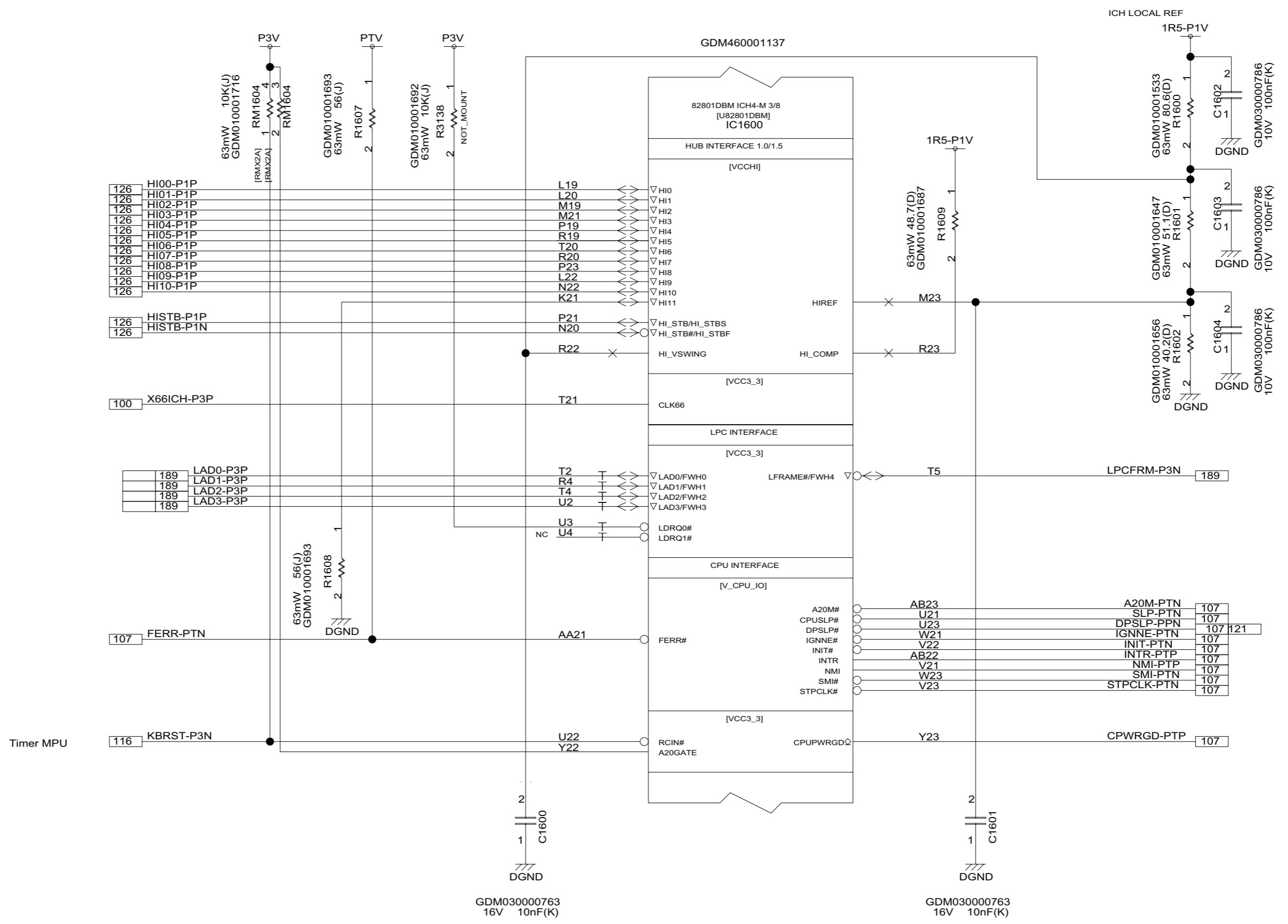
A B C D E



SCHEMATIC DIAGRAM-50

ICH4 SECTION-M3

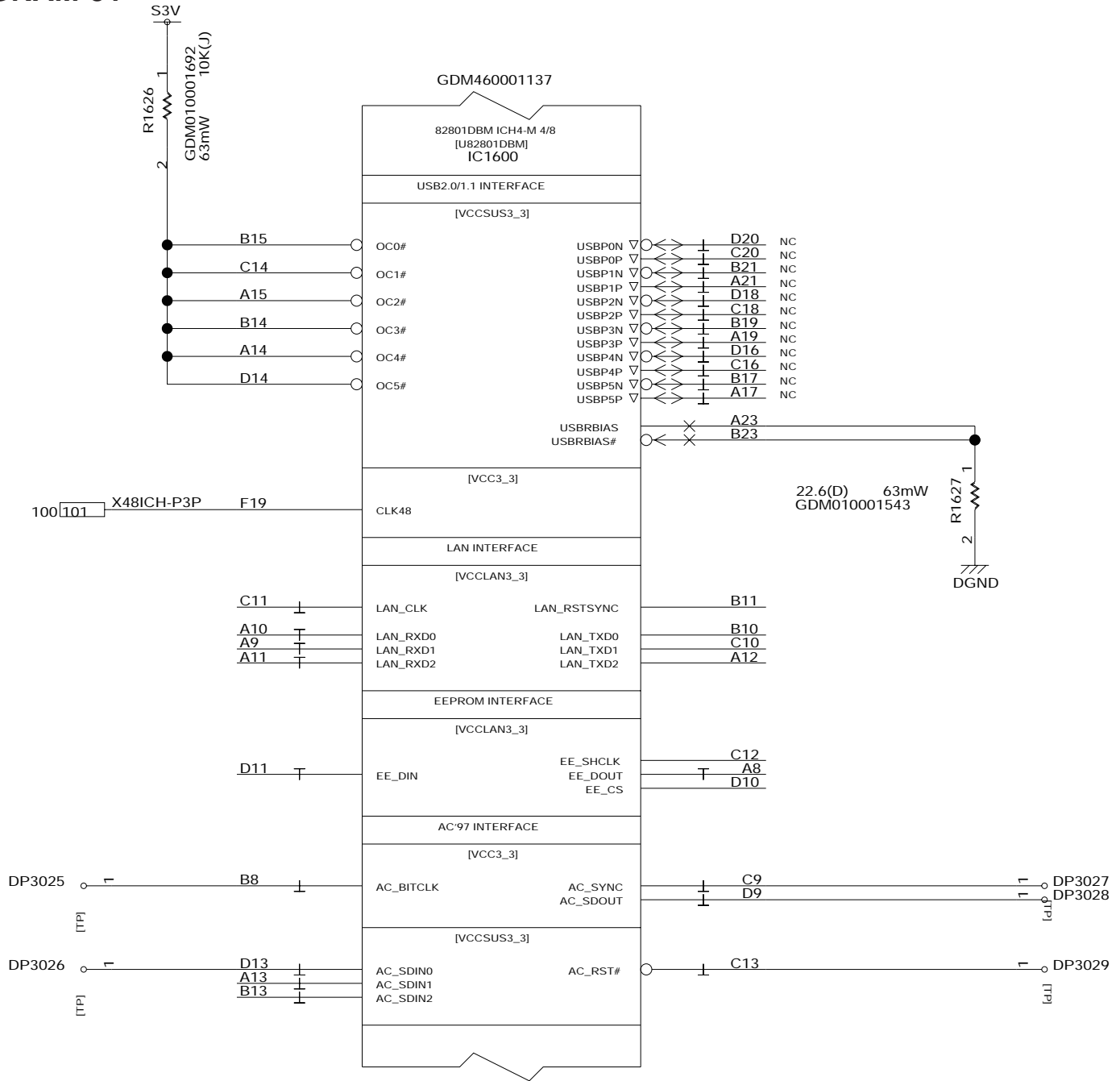
1
2
3
4
5



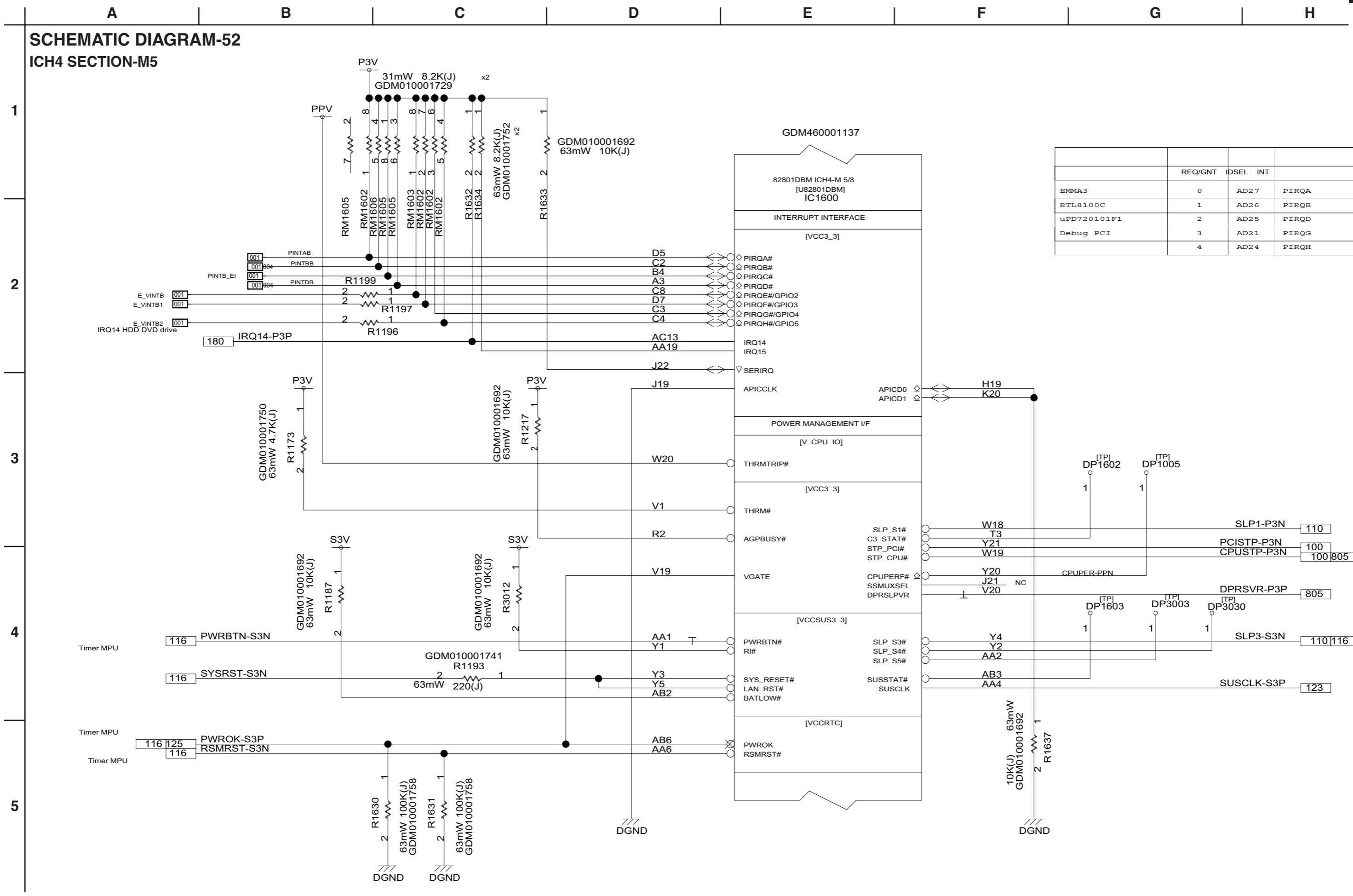
SCHEMATIC DIAGRAM-51
ICH4 SECTION-M4

1
2
3
4

A B C D E



SCHEMATIC DIAGRAM-52
ICH4 SECTION-M5



	REQ/GNT	DSEL	INT
EMMA3	0	AD27	PIRQA
RTL8100C	1	AD26	PIRQB
uPD720101F1	2	AD25	PIRQD
Debug PCI	3	AD21	PIRQG
	4	AD24	PIRQH

1
2
3
4
5

E_VINTB
E_VINTB1
E_VINTB2
IRQ14 HDD DVD drive

PINTAB
PINTBB
PINTDB
001
001
001
001
180

116 PWRBTN-S3N
116 SYSRST-S3N

116 125
116 PWROK-S3P
RSMRST-S3N

P3V
31mW 8.2K(J)
GDM010001729 x2
PPV
RM1605
RM1602
RM1606
RM1605
RM1605
RM1602
RM1602
RM1602
RM1602
R1632
R1634
R1633
63mW 8.2K(J)
GDM010001752 x2
63mW 10K(J)
R1199
R1197
R1196
GDM010001750
63mW 4.7K(J)
R1173
P3V
GDM010001692
63mW 10K(J)
R1217
P3V
GDM010001692
63mW 10K(J)
R3012
S3V
GDM010001692
63mW 10K(J)
R1187
S3V
GDM010001692
63mW 10K(J)
R3012
GDM010001741
R1193
63mW 220(J)
R1630
63mW 100K(J)
GDM010001758
R1631
63mW 100K(J)
GDM010001758
DGND
DGND

D5
C2
B4
A3
C8
D7
C3
C4
AC13
AA19
J22
J19
W20
V1
R2
V19
AA1
Y1
Y3
Y5
AB2
AB6
AA6
DGND

GDM460001137

82801DBM ICH4-M 5/8
[U82801DBM]
IC1600

INTERRUPT INTERFACE

[VCC3_3]

PIRQA#
PIRQB#
PIRQC#
PIRQD#
PIRQE#/GPIO2
PIRQF#/GPIO3
PIRQG#/GPIO4
PIRQH#/GPIO5

IRQ14
IRQ15

SERIRQ

APICCLK

APICD0
APICD1

POWER MANAGEMENT I/F

[V_CPU_IO]

THRMTRIP#

[VCC3_3]

THRM#

AGPBUSY#

VGATE

SLP_S1#
C3_STAT#
STP_PCI#
STP_CPU#
CPUPERF#
SSMUXSEL
DPRSLPVR

W18
T3
Y21
W19
Y20
J21
V20

NC

[VCCSUS3_3]

PWRBTN#
Ri#
SYS_RESET#
LAN_RST#
BATLOW#

SUSSTAT#
SUSCLK

[VCCRTC]

PWROK
RSMRST#

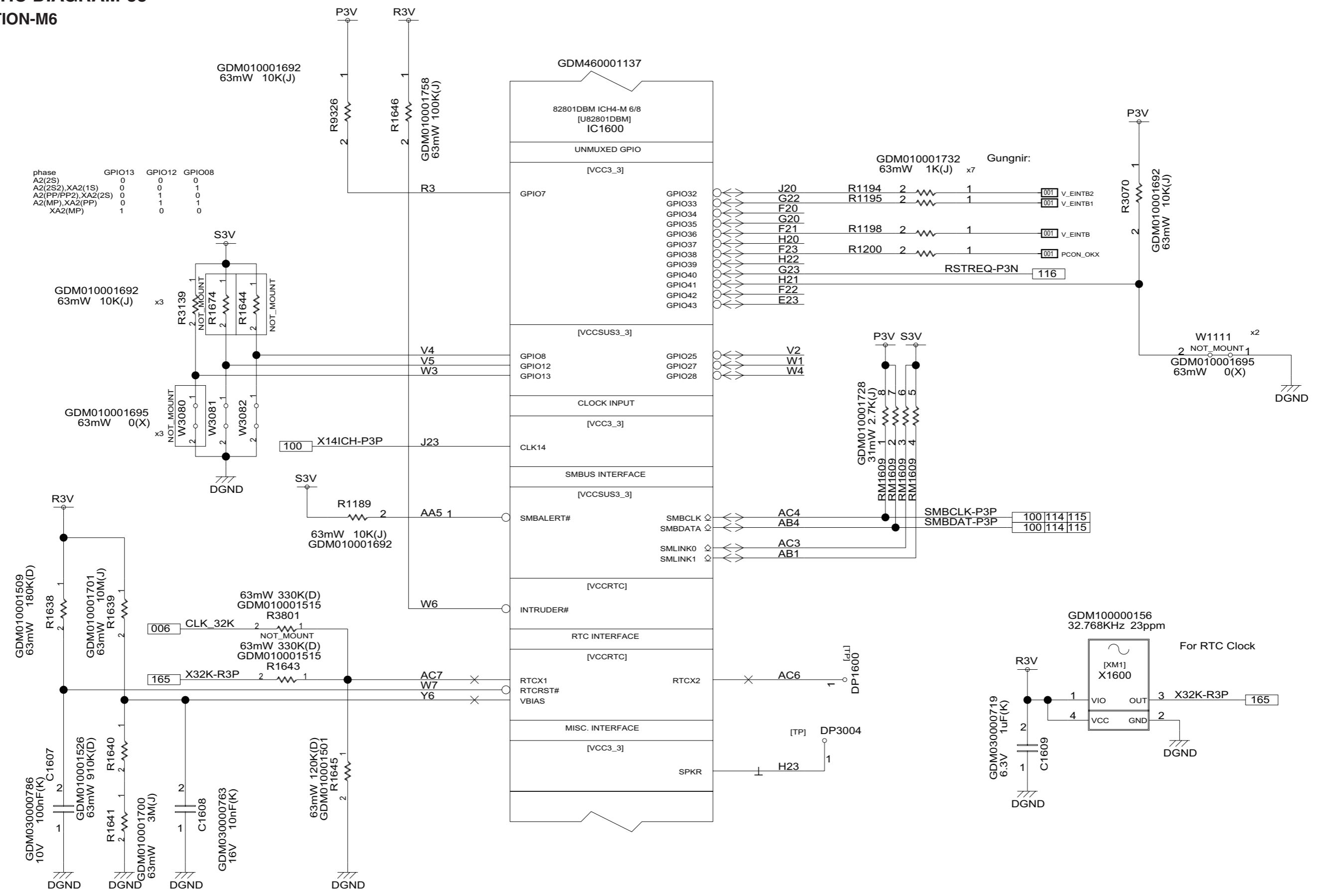
H19
K20
DP1602 [TP]
DP1005 [TP]
SLP1-P3N 110
PCISTP-P3N 100
CPUSTP-P3N 100 805
CPUPER-PPN
DPRSVR-P3P 805
DP1603 [TP]
DP3003 [TP]
DP3030 [TP]
SLP3-S3N 110 116
SUSCLK-S3P 123
R1637
63mW
10K(J)
GDM010001692
DGND

Timer MPU
Timer MPU
Timer MPU

SCHEMATIC DIAGRAM-53 ICH4 SECTION-M6

phase	GPIO13	GPIO12	GPIO08
A2(2S)	0	0	0
A2(2S2),XA2(1S)	0	0	1
A2(PP/PP2),XA2(2S)	0	1	0
A2(MP),XA2(PP)	0	1	1
XA2(MP)	1	0	0

1
2
3
4
5

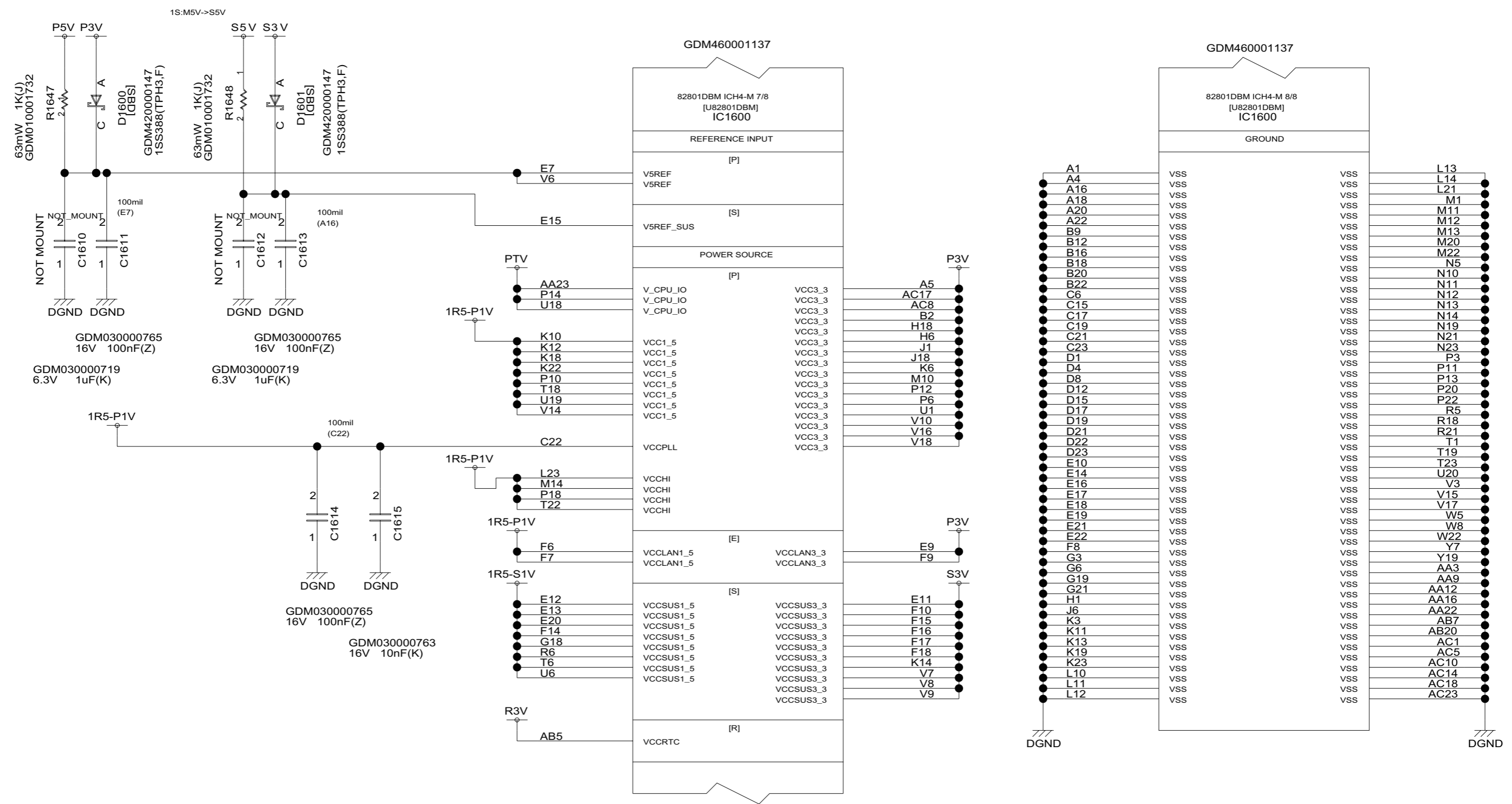


SCHEMATIC DIAGRAM-54

ICH4 SECTION-M7

1
2
3
4
5

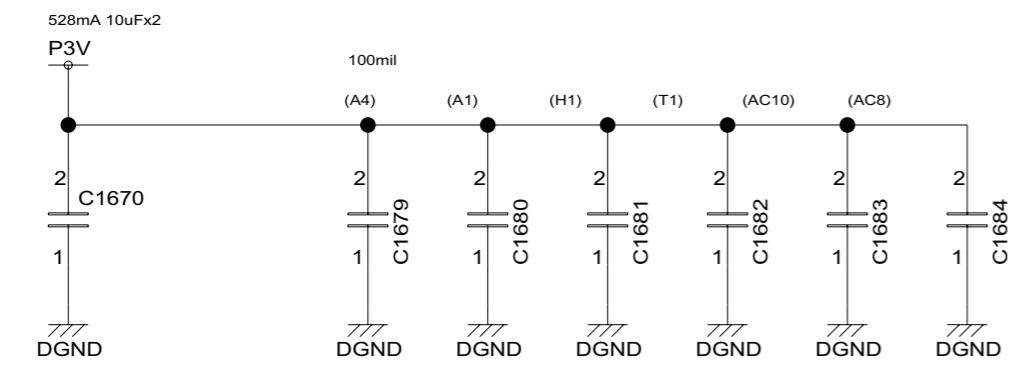
A B C D E F G H



A B C D E F G H

SCHEMATIC DIAGRAM-55
ICH4 SECTION-M8

1



GDM030000758
6.3V 22uF(K)

GDM030000765
16V 100nF(Z)

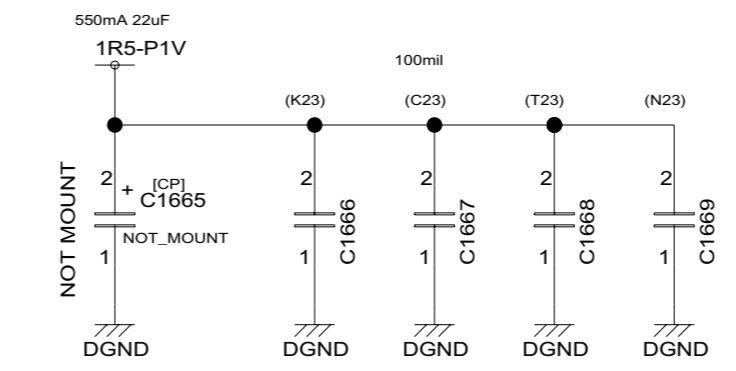
GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)



GDM030000829
4V 150uF(M)

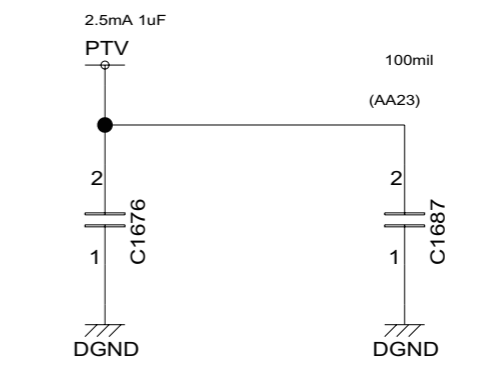
GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)

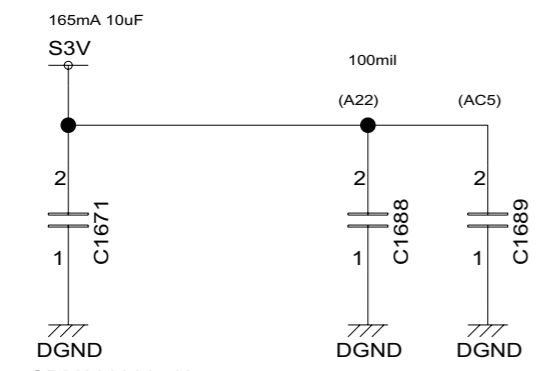
GDM030000765
16V 100nF(Z)



GDM030000719
6.3V 1uF(K)

GDM030000765
16V 100nF(Z)

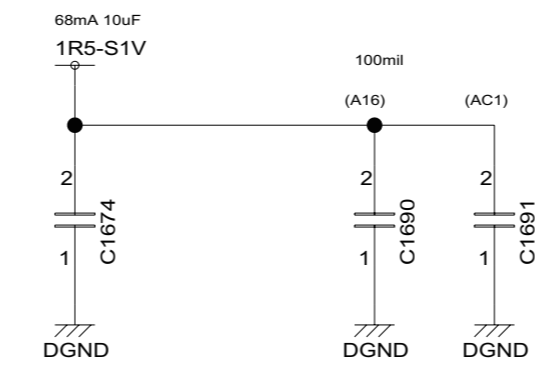
2



GDM030000748
6.3V 10uF(K)

GDM030000765
16V 100nF(Z)

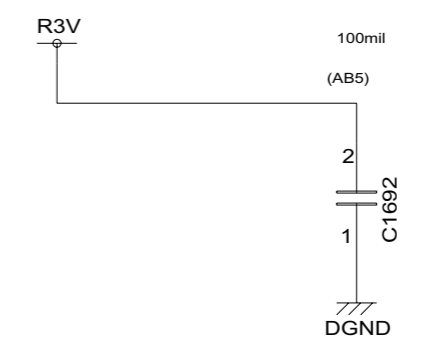
GDM030000765
16V 100nF(Z)



GDM030000657
6.3V 4.7uF(K)

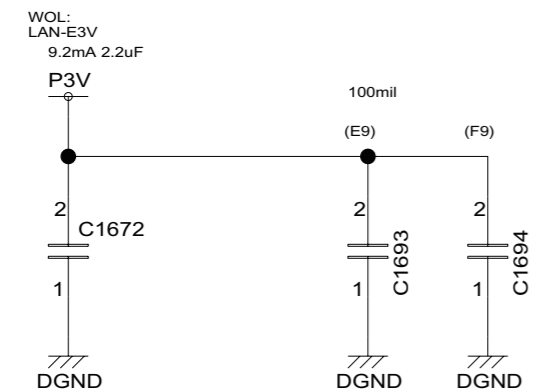
GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)



GDM030000765
16V 100nF(Z)

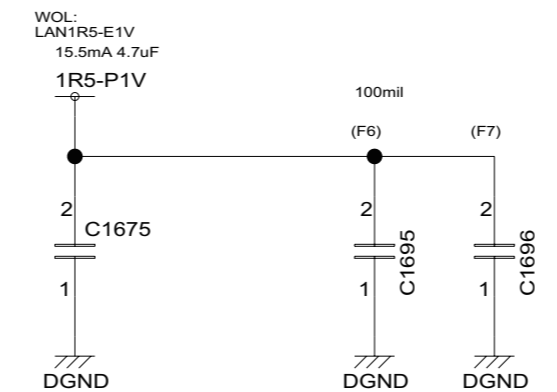
3



GDM030000657
6.3V 4.7uF(K)

GDM030000765
16V 100nF(Z)

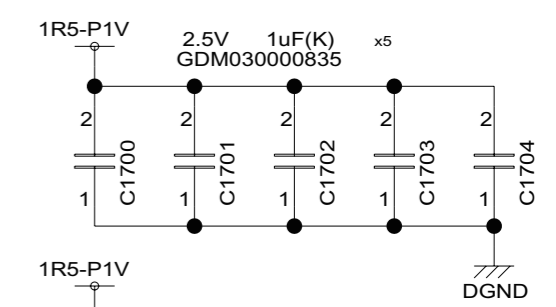
GDM030000765
16V 100nF(Z)



GDM030000657
6.3V 4.7uF(K)

GDM030000765
16V 100nF(Z)

GDM030000765
16V 100nF(Z)



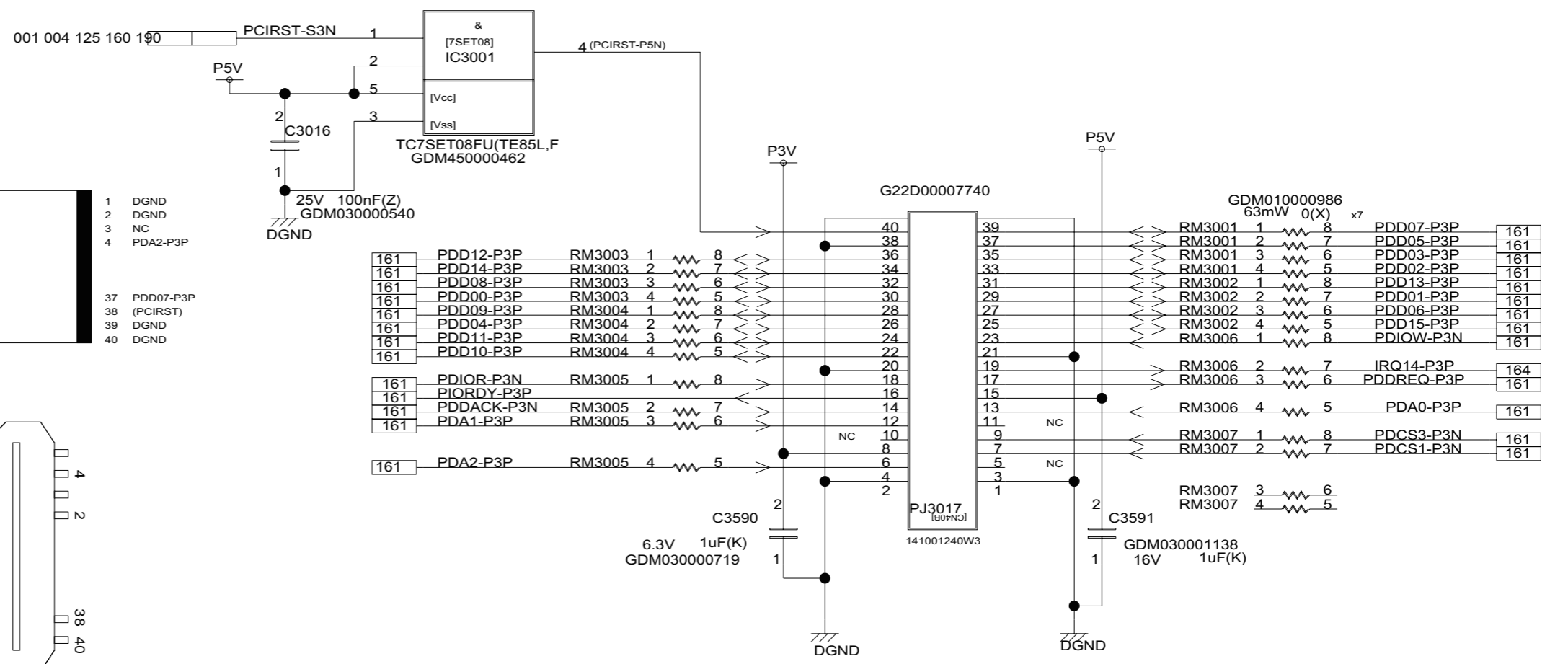
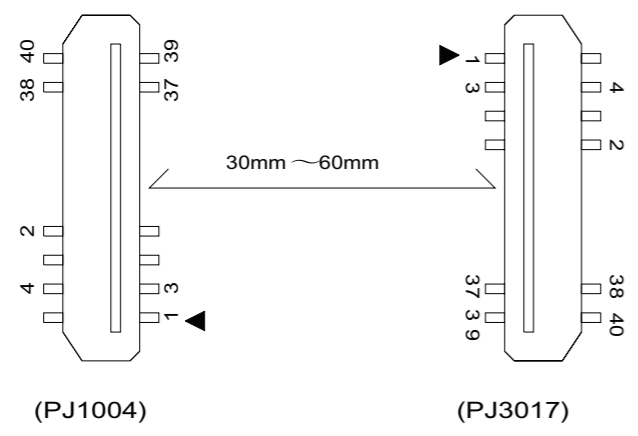
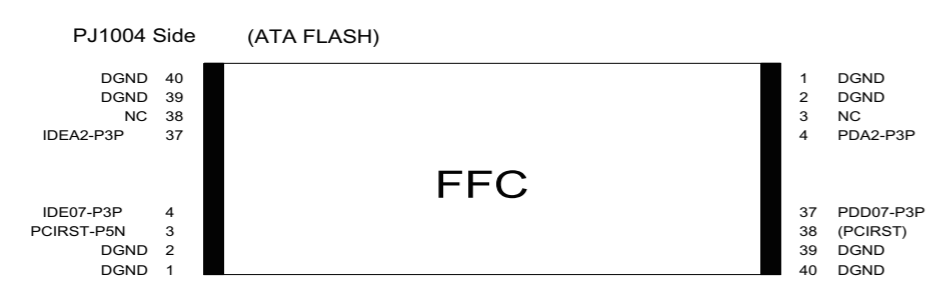
GDM030000765
16V 100nF(Z)

4

5

SCHEMATIC DIAGRAM-56
IDE I/F SECTION

1
2
3
4
5



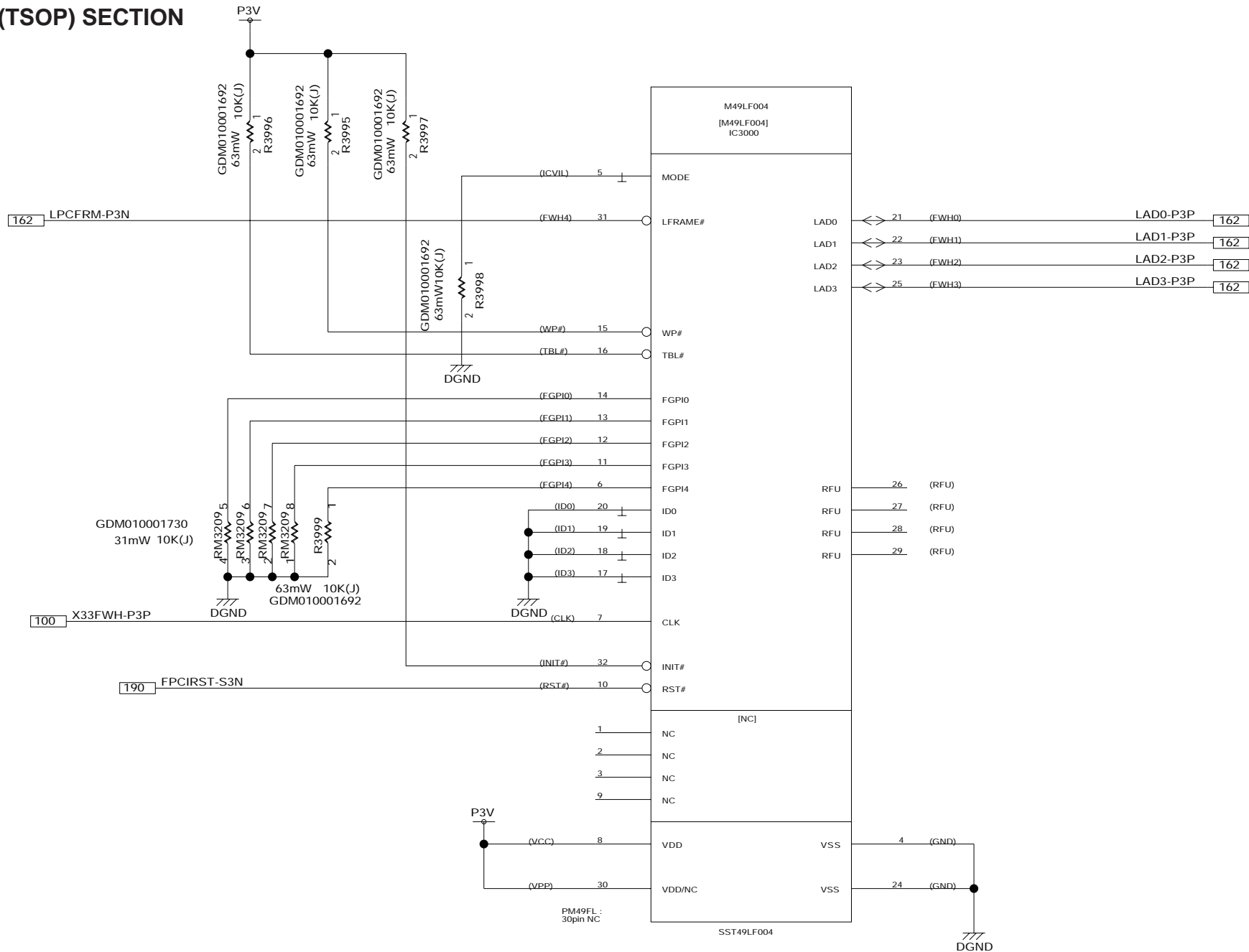
SCHEMATIC DIAGRAM-57
FWH (TSOP) SECTION

1

2

3

4



A

B

C

D

E

SCHEMATIC DIAGRAM-58

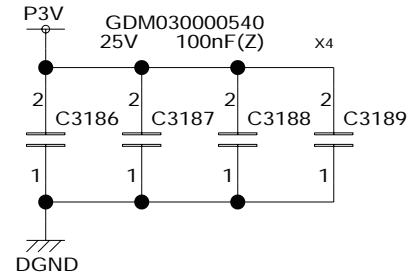
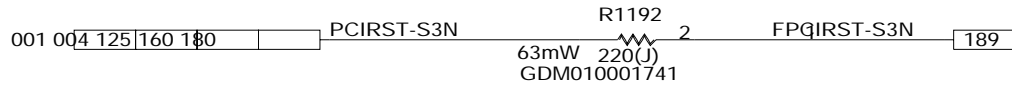
FWH SECTION

1

2

3

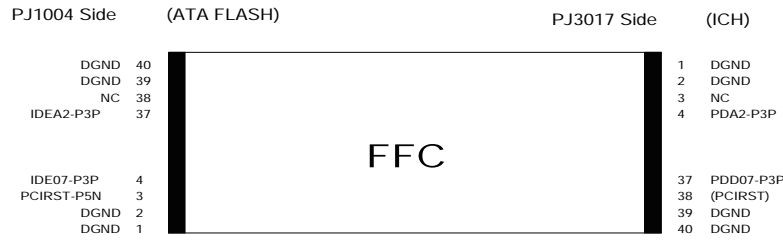
4



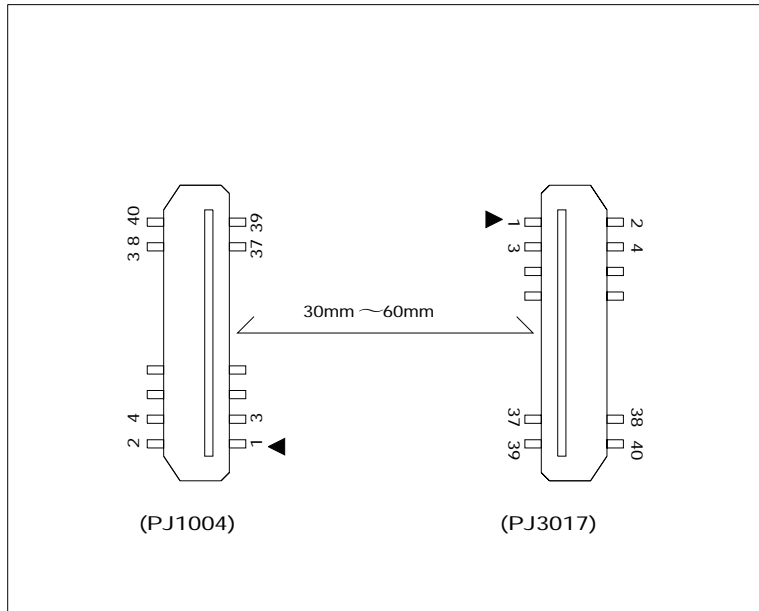
SCHEMATIC DIAGRAM-59

ATA FLASH I/F

1



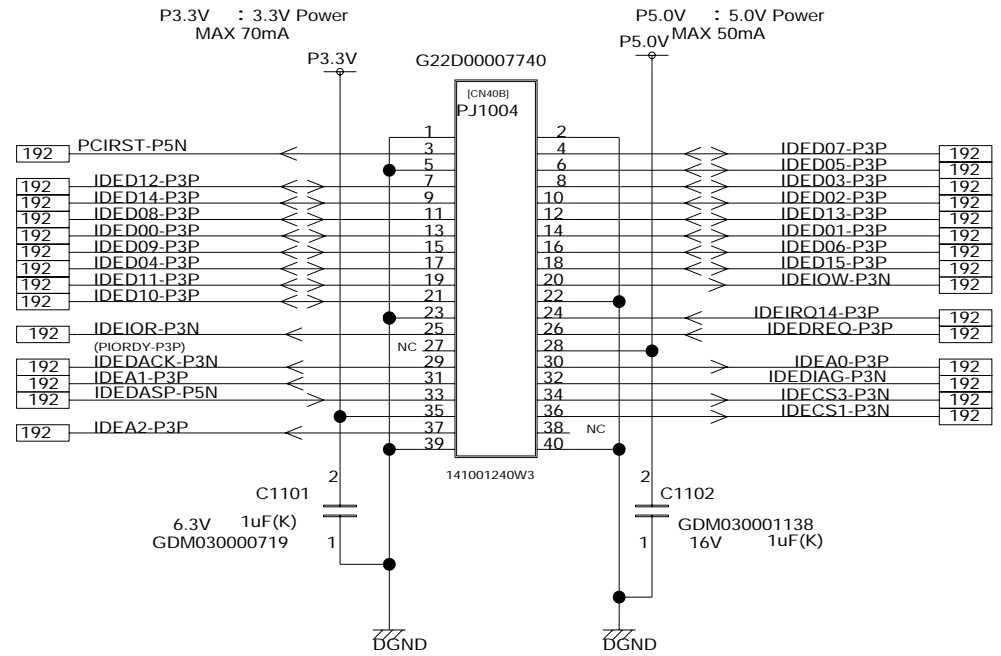
2



3

4

ATA FLASH



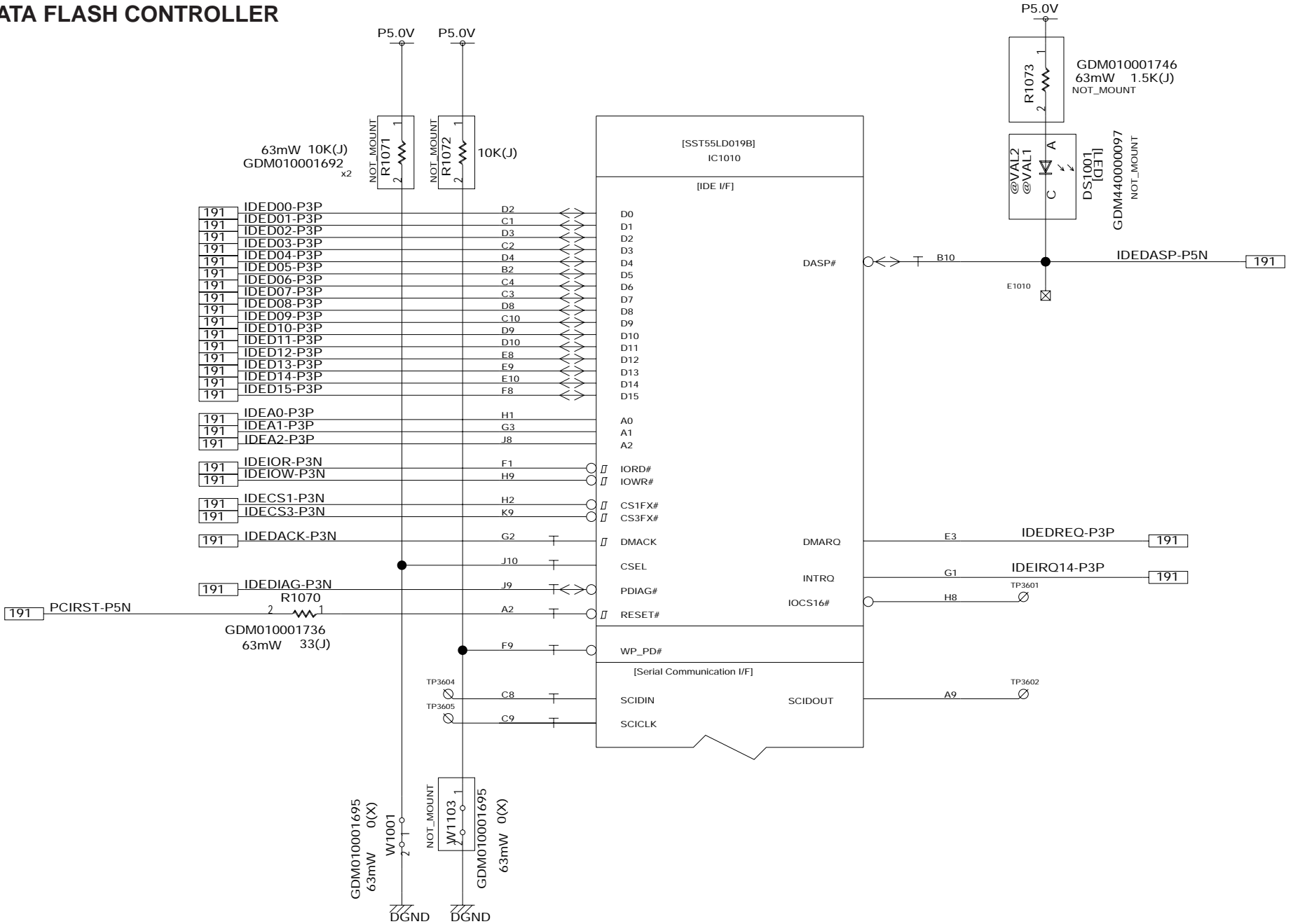
SCHEMATIC DIAGRAM-60 ATA FLASH CONTROLLER

1

2

3

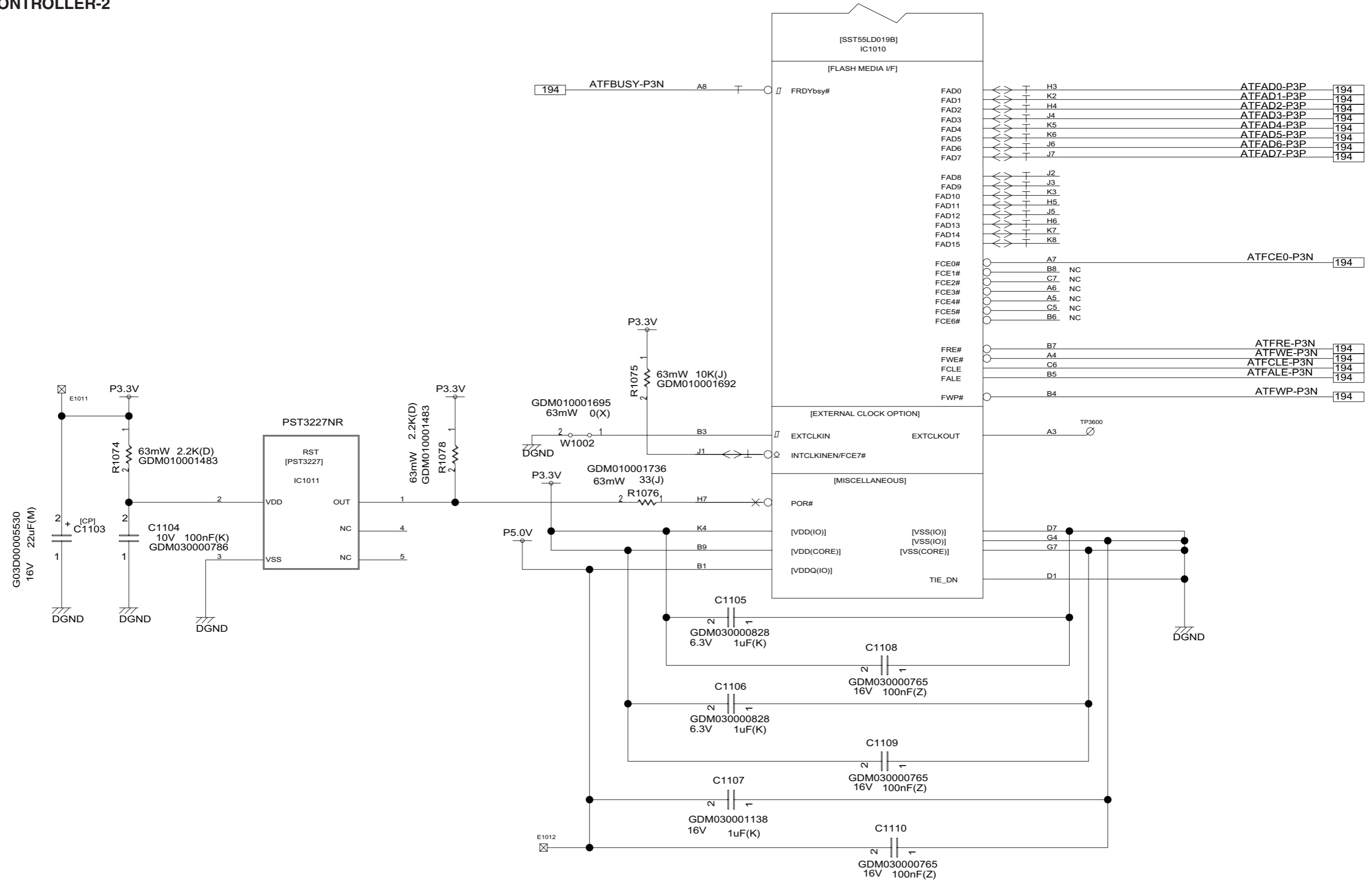
4



SCHEMATIC DIAGRAM-61 ATA FLASH CONTROLLER-2

1
2
3
4
5

A B C D E F G H



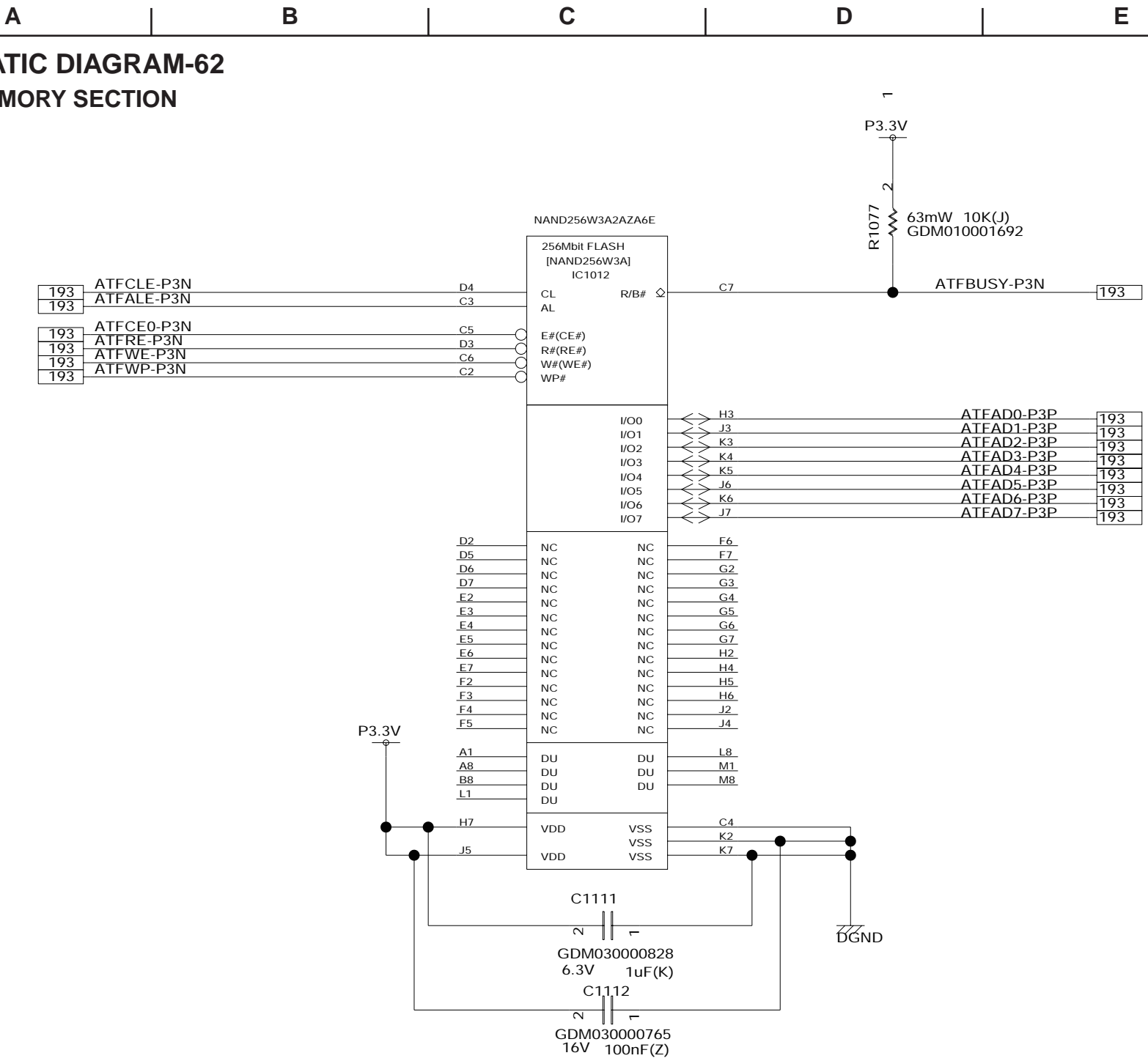
SCHEMATIC DIAGRAM-62
NAND MEMORY SECTION

1

2

3

4



A

B

C

D

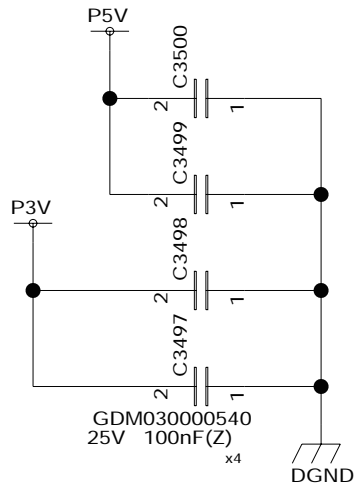
E

SCHEMATIC DIAGRAM-63

DEBUG PCI AND KINNERETH

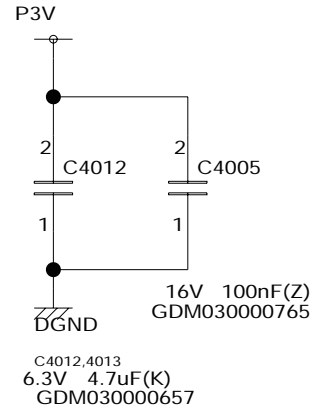
1

Debug PCI



2

KINNERETH



3

4

SCHEMATIC DIAGRAM-64

USB I/F

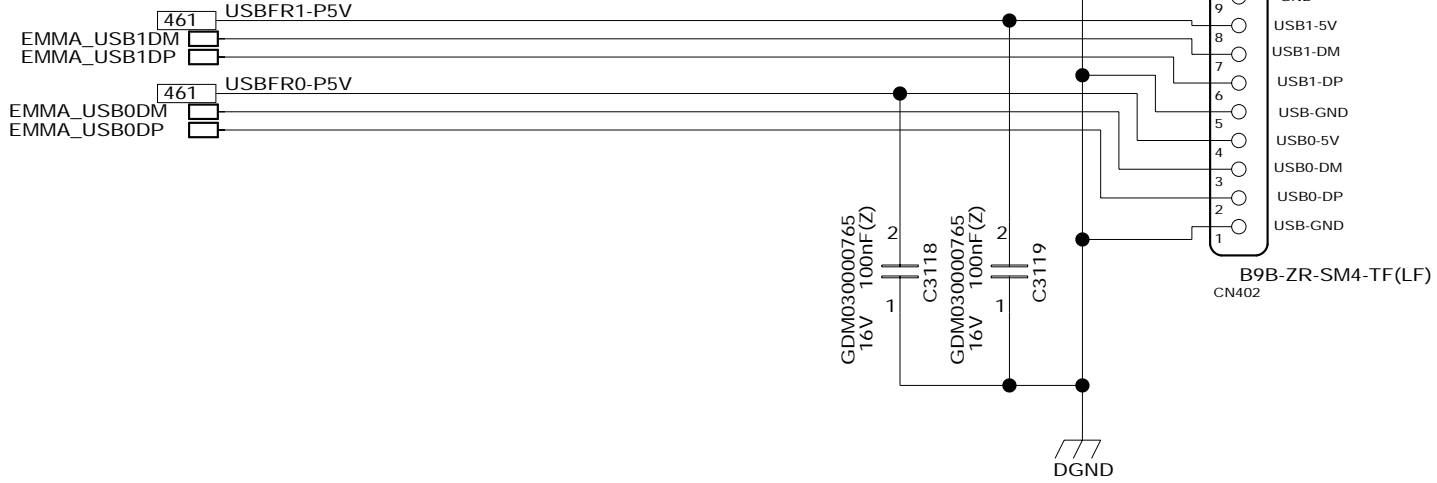
**USB I/F AND
USB POWER**

1

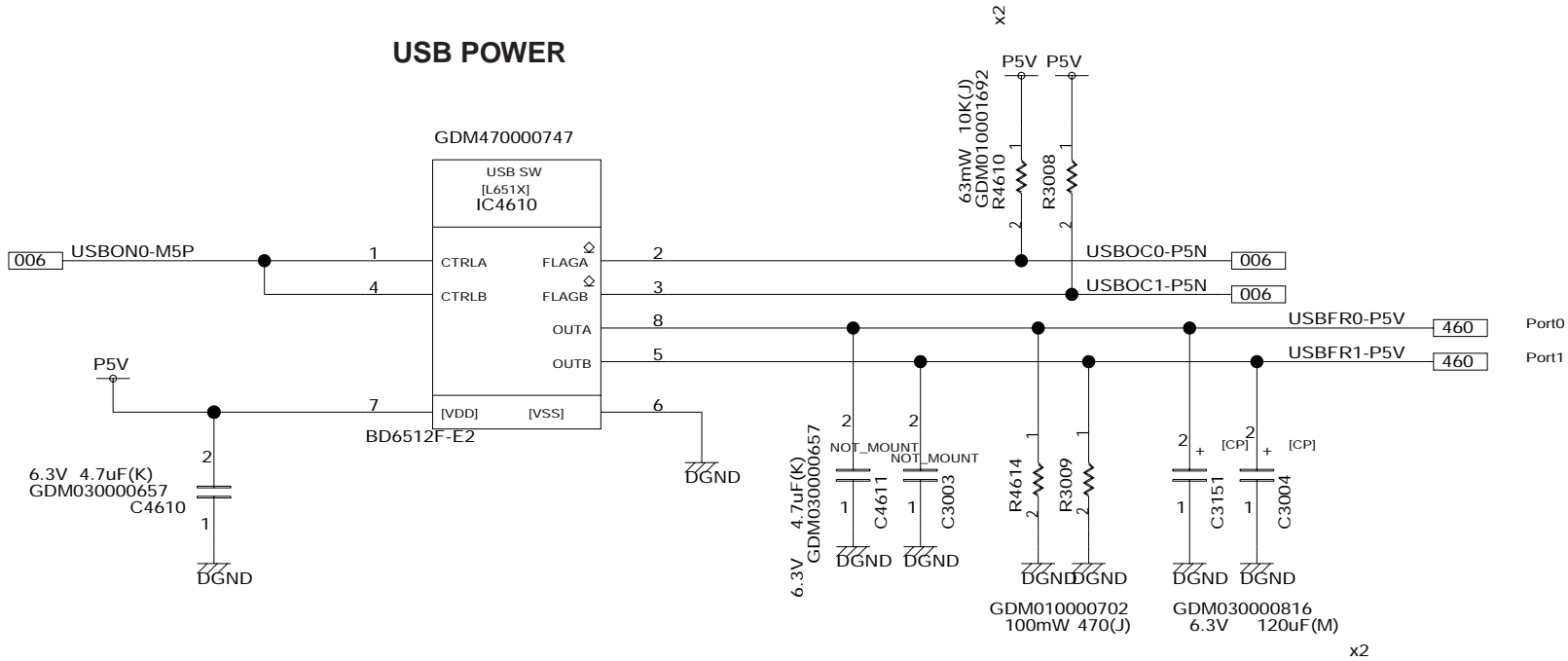
2

3

4



USB POWER



x2

A

B

C

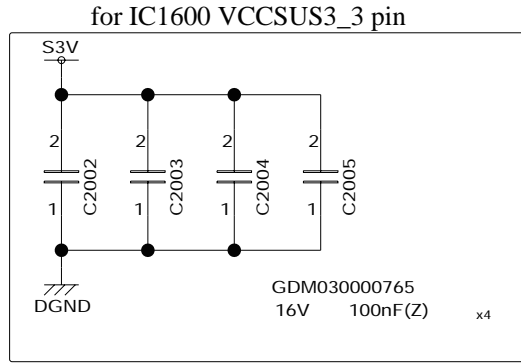
D

E

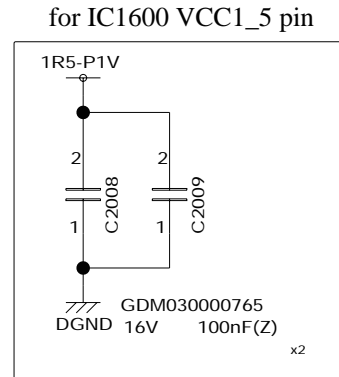
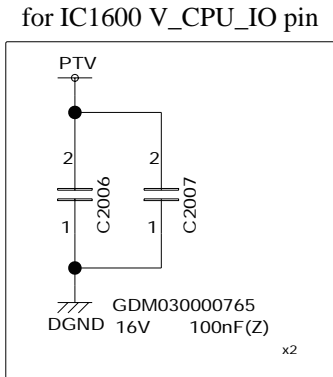
SCHEMATIC DUAGRAM-65

ADDITIONAL CAPACITOR-3

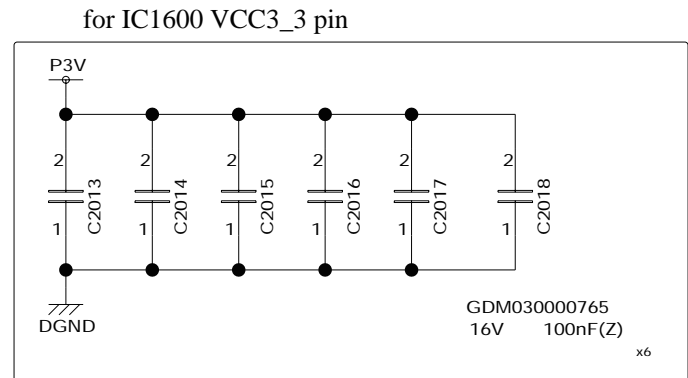
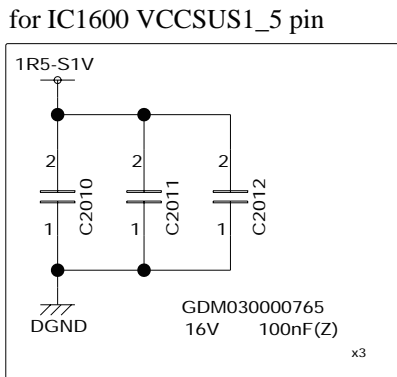
1



2



3



4

SCHEMATIC DIAGRAM-66 PS CONNECTOR

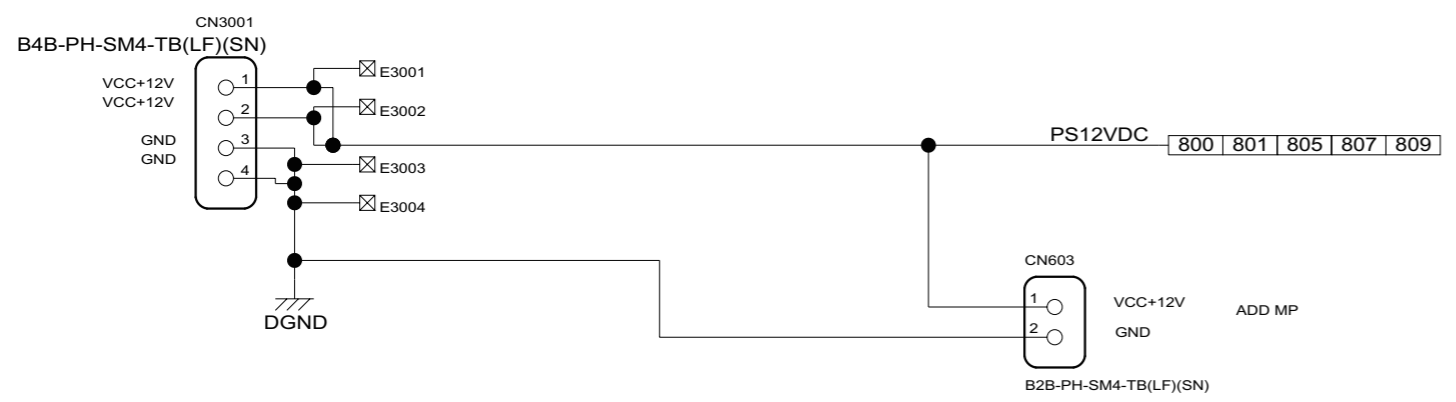
1

2

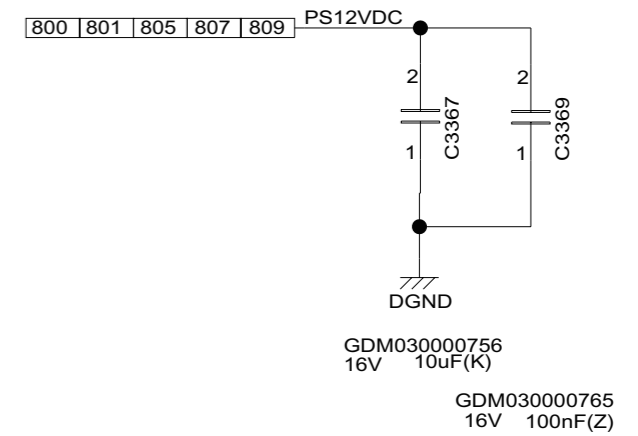
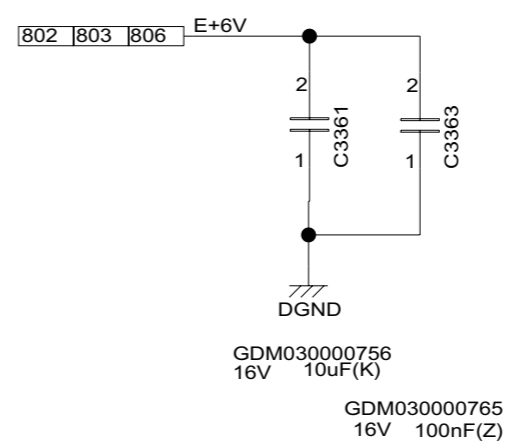
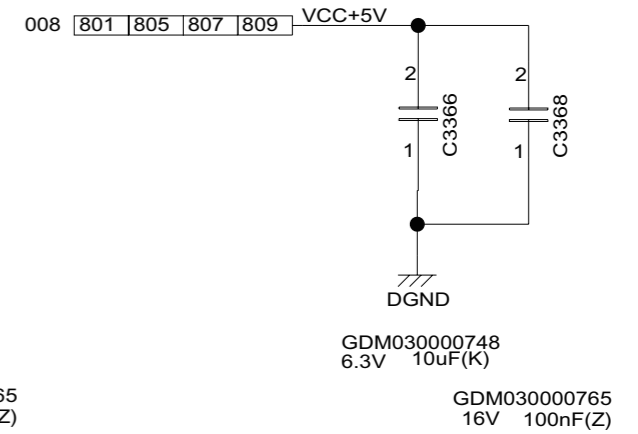
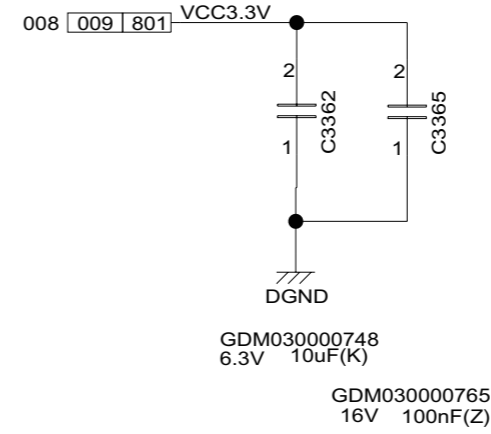
3

4

5



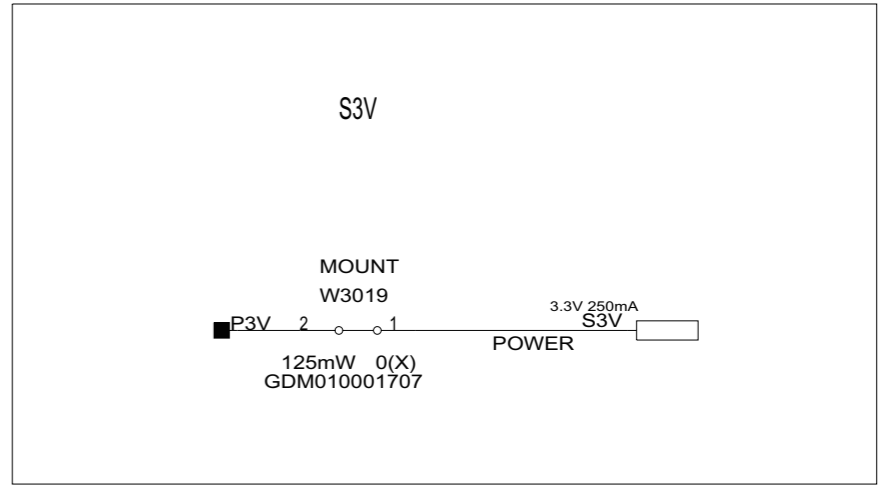
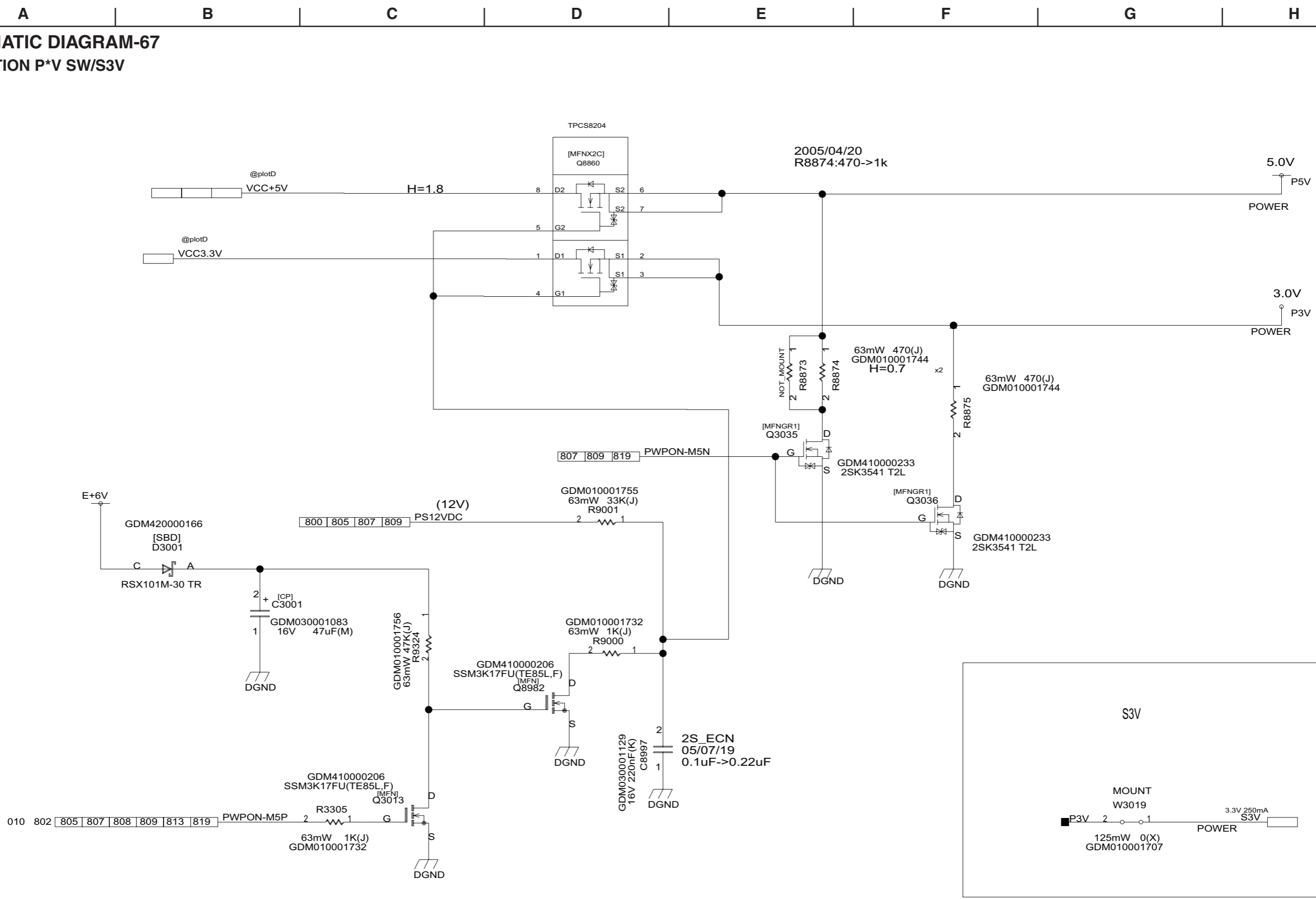
- VCC+5V PS5VDC
- VCC3.3V PS3VDC
- E+6V PS5VSB



SCHEMATIC DIAGRAM-67

PS SECTION P*V SW/S3V

1
2
3
4
5



A

B

C

D

E

SCHEMATIC DIAGRAM-68

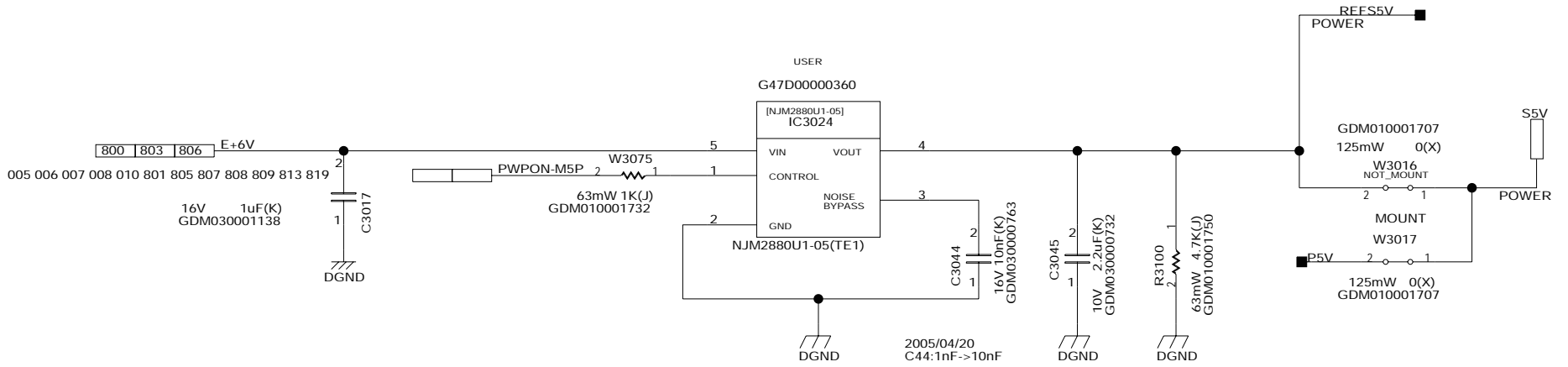
PS SECTION S5V

1

2

3

4



A

B

C

D

E

SCHEMATIC DIAGRAM-69

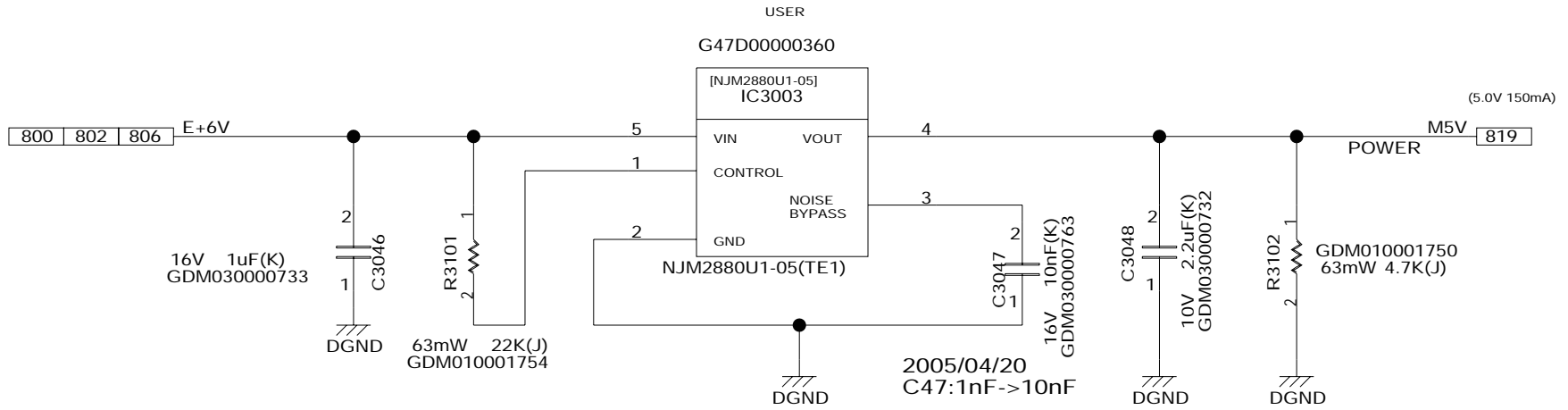
PS SECTION M5V

1

2

3

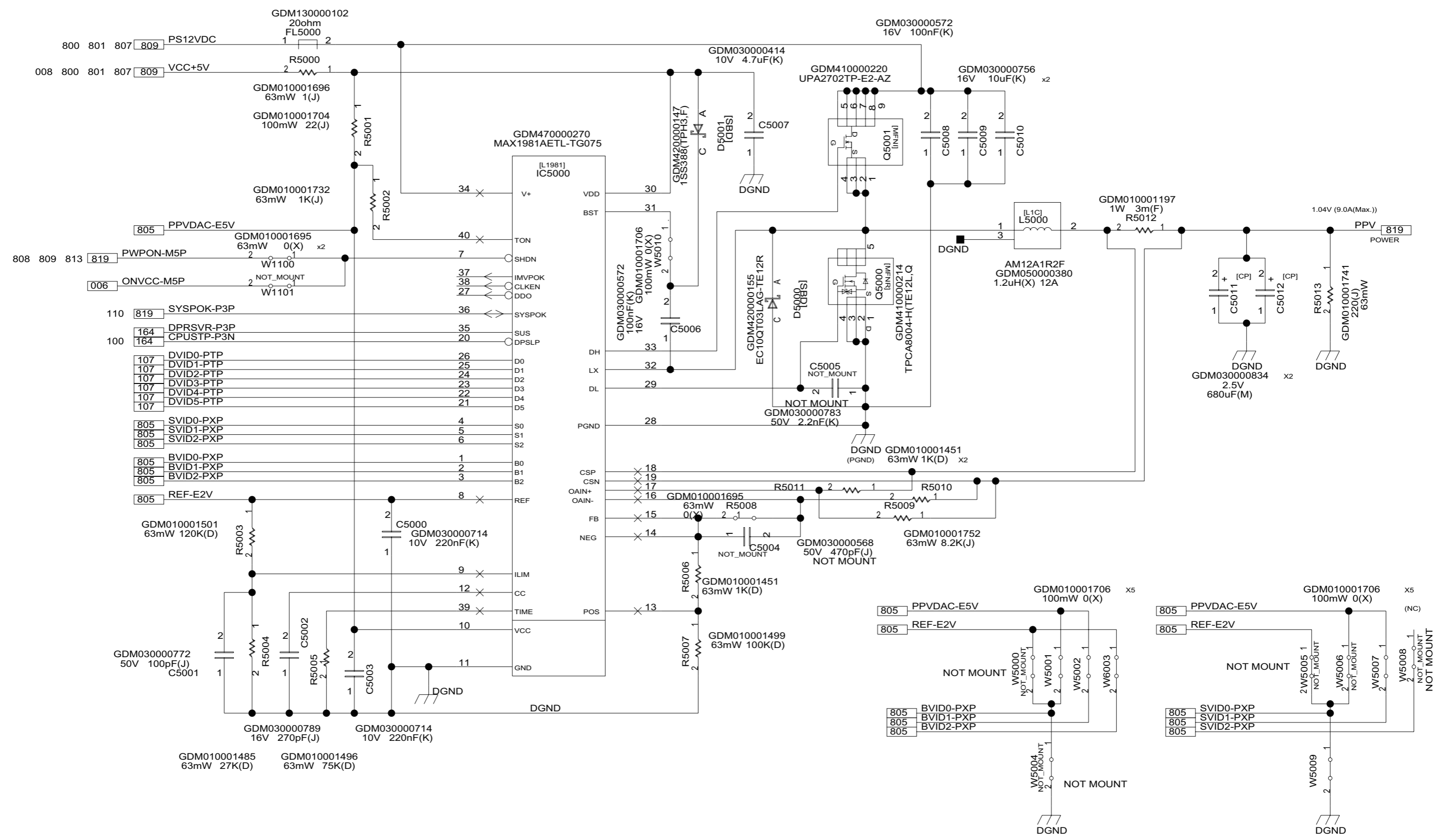
4



SCHEMATIC DIAGRAM-70

PS SECTION PPV

1
2
3
4
5



A

B

C

D

E

SCHEMATIC DIAGRAM-71

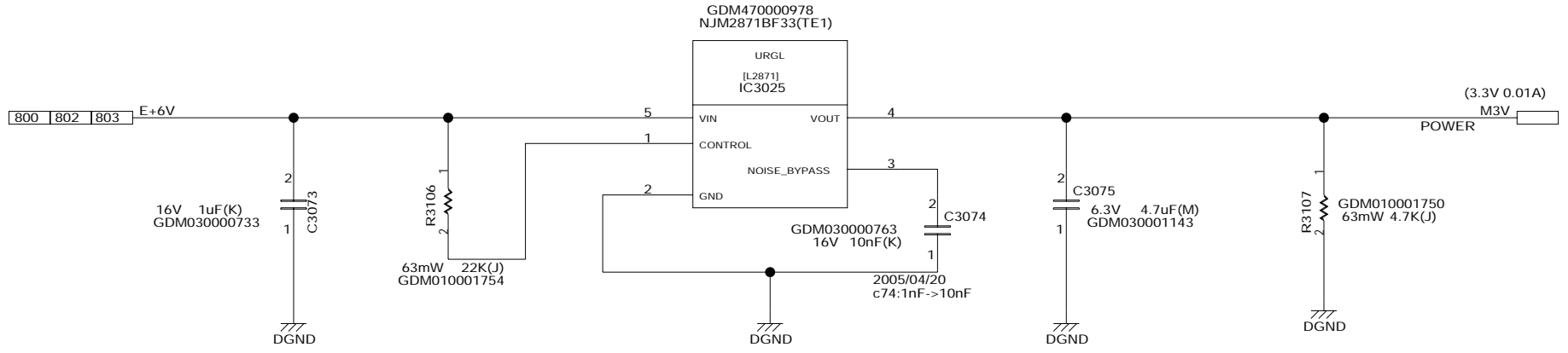
PS SECTION M3V

1

2

3

4



SCHEMATIC DIAGRAM-72

PS SECTION 2R5-P2V

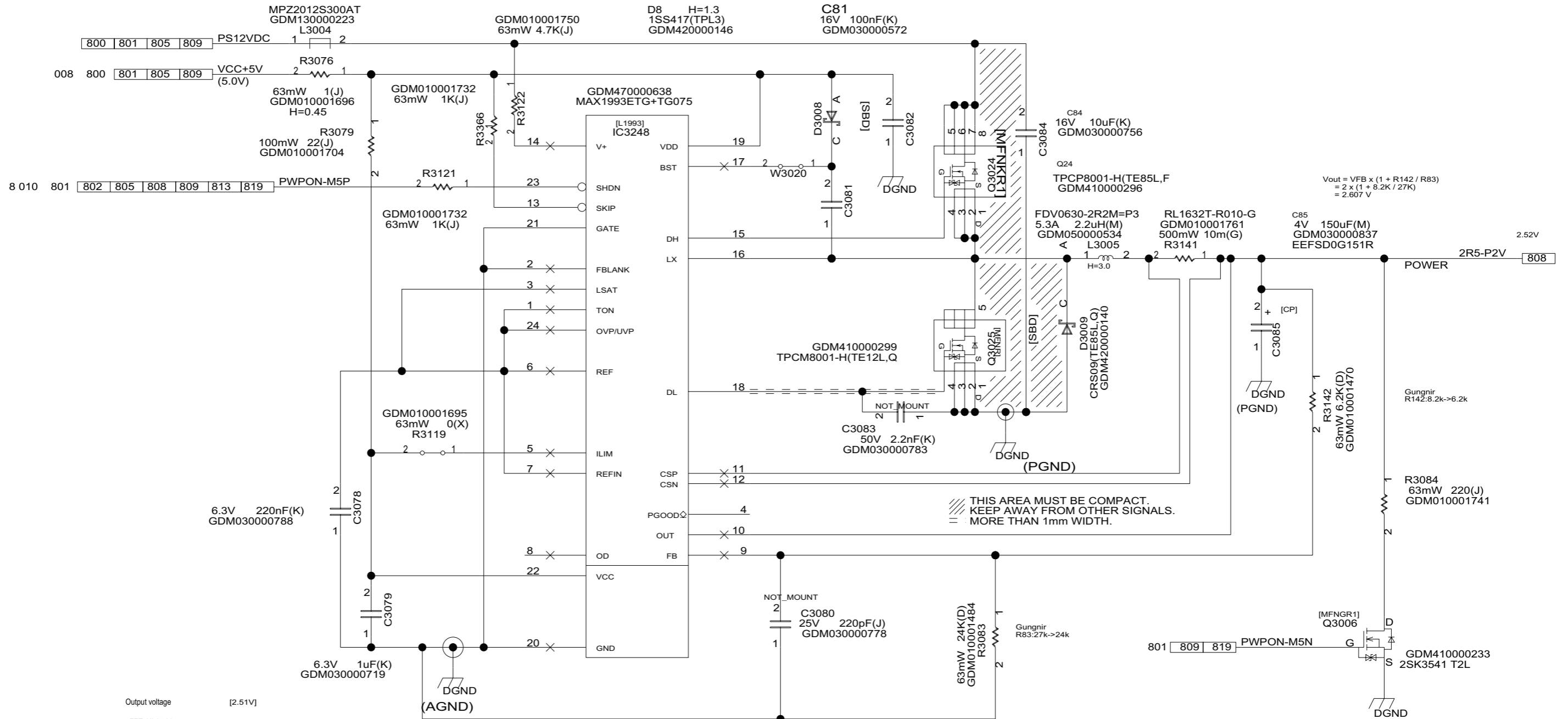
Operating FREQ. : TON = REF [450KHz]
 Low Noise Mode : SKIP = PVON [Enable]
 Current Limit : ILIMIT [6.7A (Min)]
 [7.7A (Typ)]
 [8.7A (Max)]
 FeedBack Voltage; 1.0 V(Typ.)
 OV Protection : Disable
 UV Protection : Enable
 Latch : Disable

W? H=1.3
 100mW 0(X)
 GDM010001706

D8 H=1.3
 1SS417(TPL3)
 GDM420000146

C82 H=1.15
 6.3V 1uF(K)
 GDM030000719

C81
 16V 100nF(K)
 GDM030000572



$$V_{out} = V_{FB} \times (1 + R_{142} / R_{83})$$

$$= 2 \times (1 + 8.2K / 27K)$$

$$= 2.607 V$$

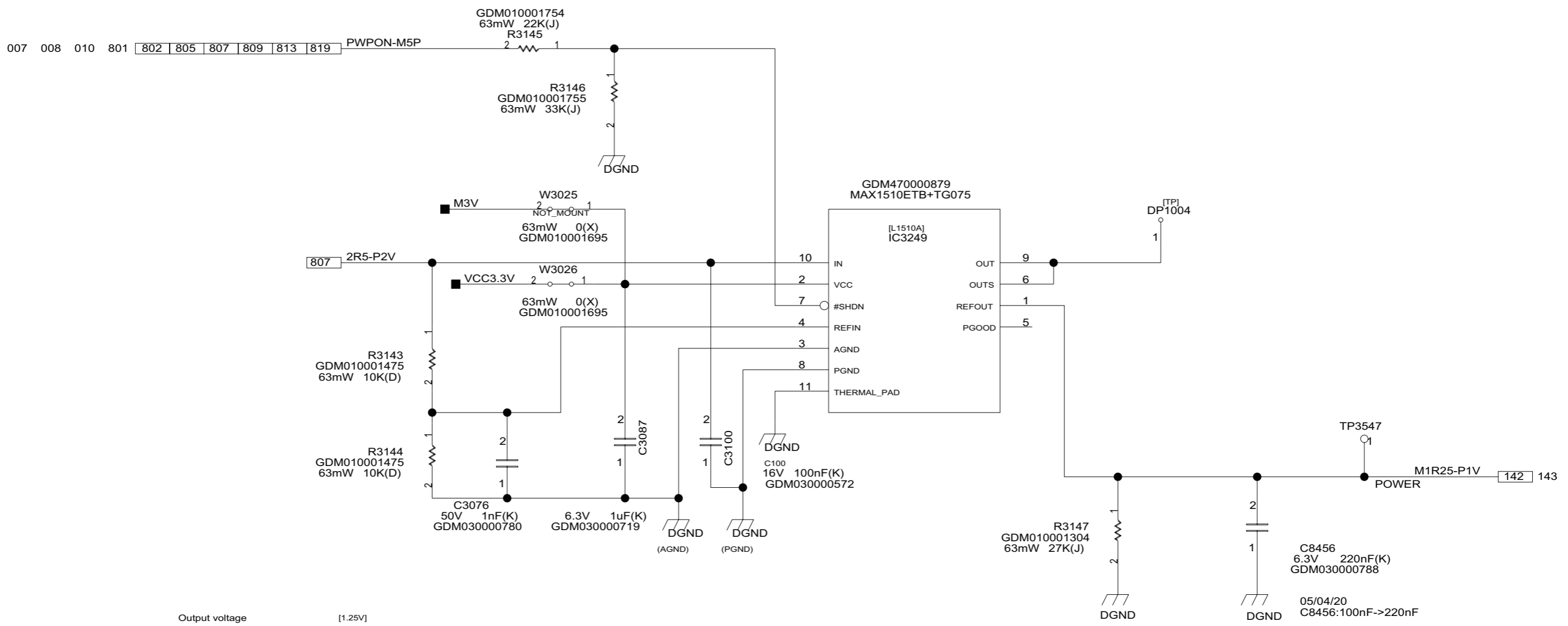
THIS AREA MUST BE COMPACT.
 KEEP AWAY FROM OTHER SIGNALS.
 MORE THAN 1mm WIDTH.

Output voltage [2.51V]
 FET High side [TPC8010-H]
 Low side [TPC8010-H]
 Capacitor [4.0V 150UF 7m]
 Coil [C10-H3.5R2R2]
 Diode [1.0A]
 Power control signal [BVON-S5P]
 Skip mode [PVON-S5P]
 Pull circuit [220ohm]
 Overcurrent limiter [7.7A]

1
 2
 3
 4
 5

SCHEMATIC DIAGRAM-73
PS SECTION 1R25-P1V

1
2
3
4
5



Output voltage	[1.25V]
FET	[UPA2752GR]
Input capacitor	[4.0V 150UF 30m]
Output capacitor	[4.0V 150UF 30m]
Coil	[A916BY-1R2M=P3]
Diode	[0.5A]
Output power control	[PVON-S5P]
Skip mode	[N/A]
Pull circuit	[220ohm]
Over current limiter	[3.5A]

05/04/20
 C8456:100nF->220nF

SCHEMATIC DIAGRAM-75

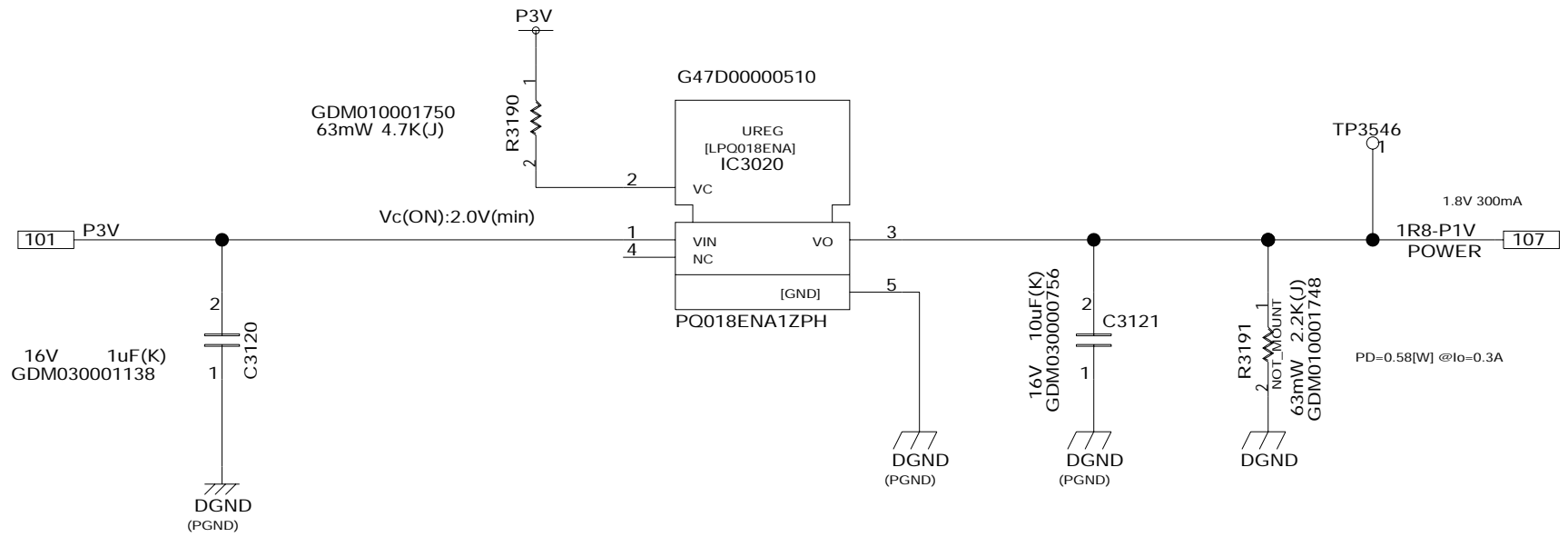
PS SECTION 1R8-P1V

1

2

3

4



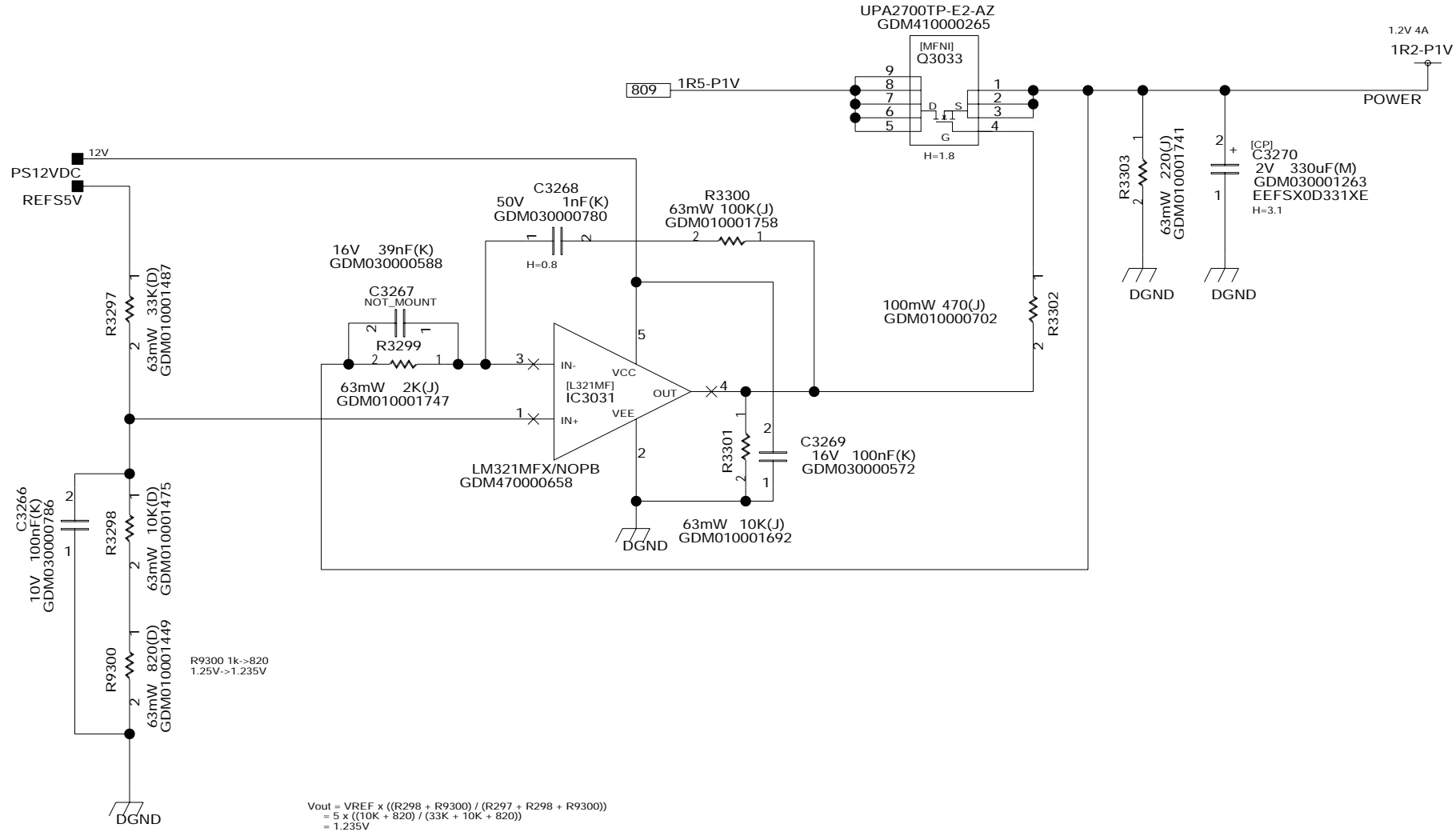
SCHEMATIC DIAGRAM-76
PS SECTION 1R2-P1V

1

2

3

4

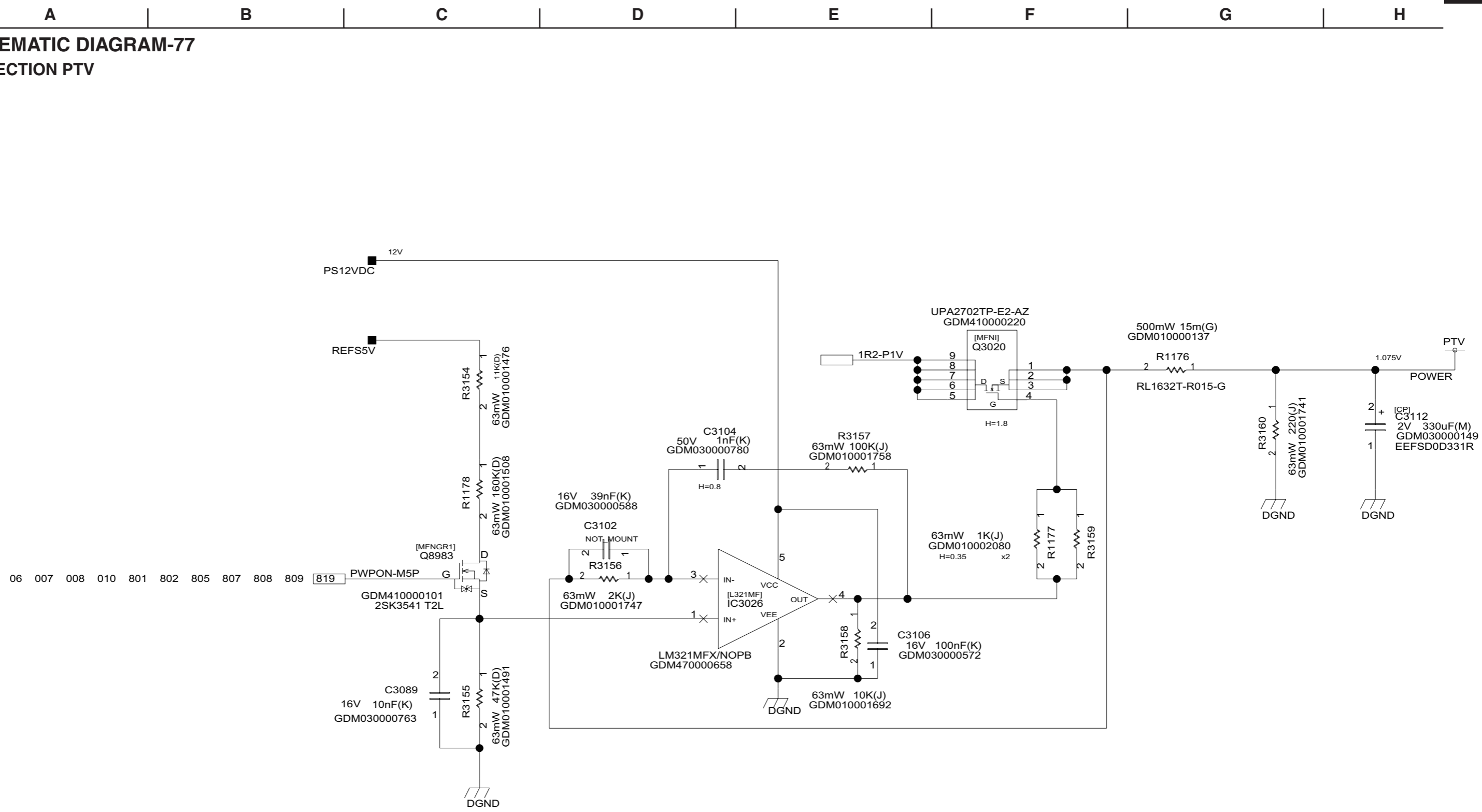


$$\begin{aligned}
 V_{out} &= V_{REF} \times ((R_{298} + R_{9300}) / (R_{297} + R_{298} + R_{9300})) \\
 &= 5 \times ((10K + 820) / (33K + 10K + 820)) \\
 &= 1.235V
 \end{aligned}$$

Output voltage [1.36V]
 FET [UPA2702TP]
 Capacitor [2.0V 330UF 7m]
 Power output control signal [PVON-SSP]
 Pull out circuit [220ohm]

SCHEMATIC DIAGRAM-77
PS SECTION PTV

1
2
3
4
5



06 007 008 010 801 802 805 807 808 809 819

A

B

C

D

E

SCHEMATIC DIAGRAM-78

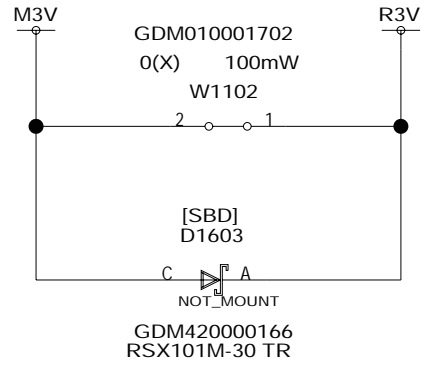
PS SECTION RTC VCC

1

2

3

4



A

B

C

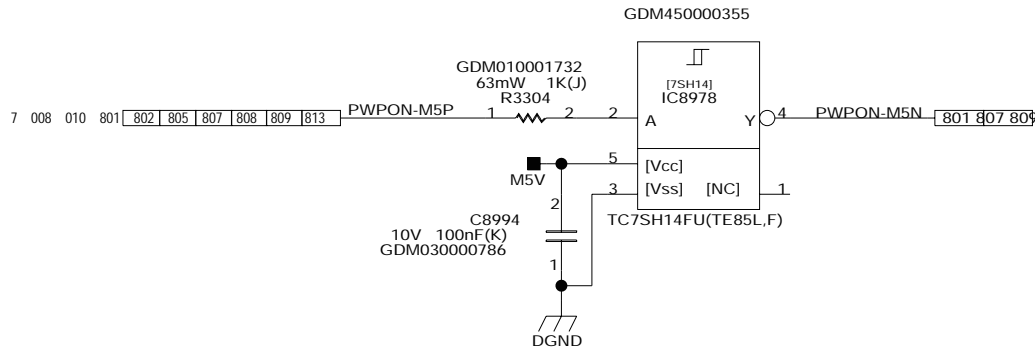
D

E

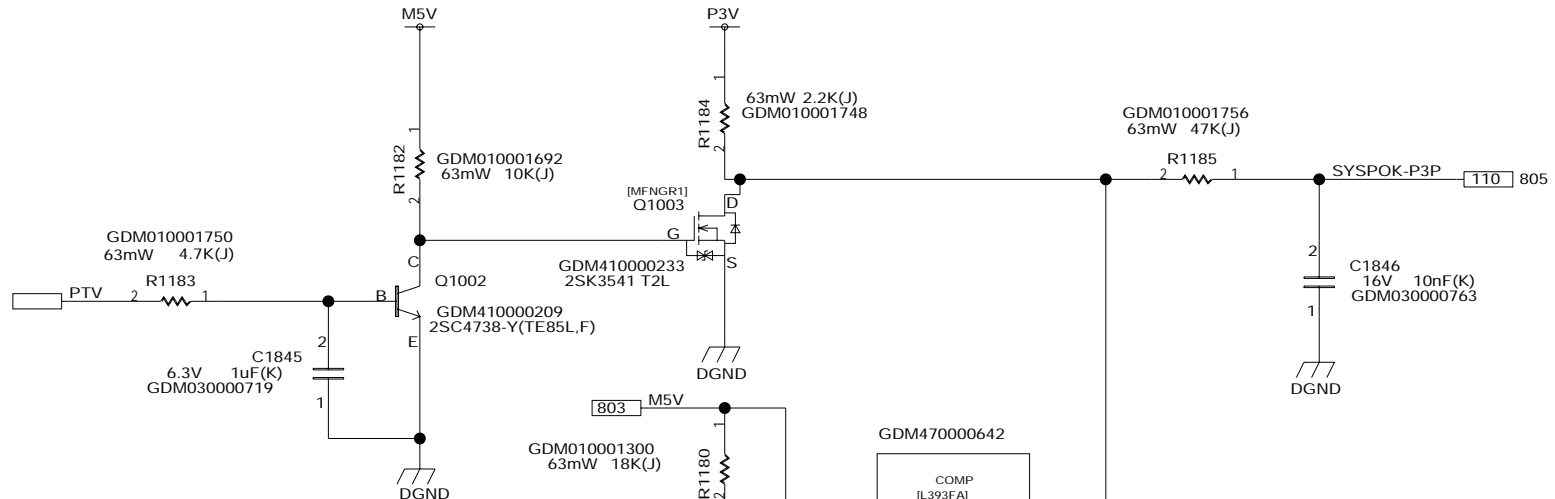
SCHEMATIC DIAGRAM-79

PS SECTION MISC

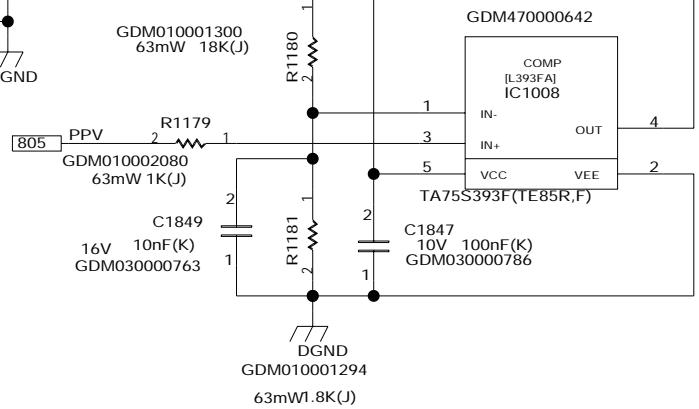
1



2



3



4

A

B

C

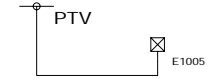
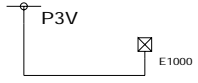
D

E

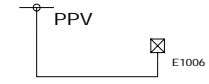
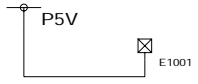
SCHEMATIC DIAGRAM-80

TEST PAD

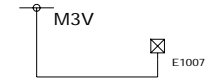
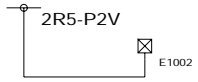
1



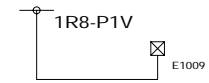
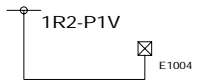
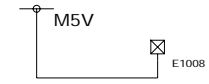
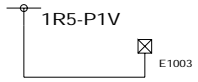
2



3



4



A B C D E F G H

SCHEMATIC DIAGRAM-81
CAPACITOR

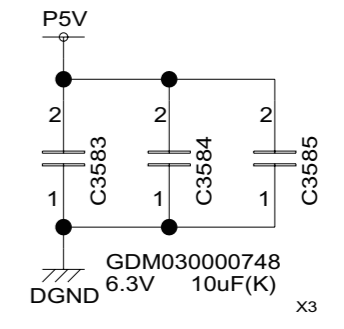
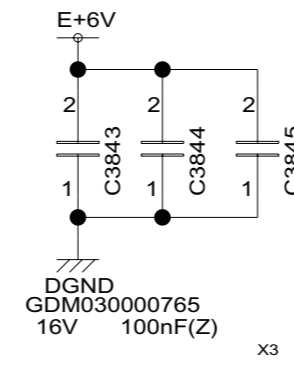
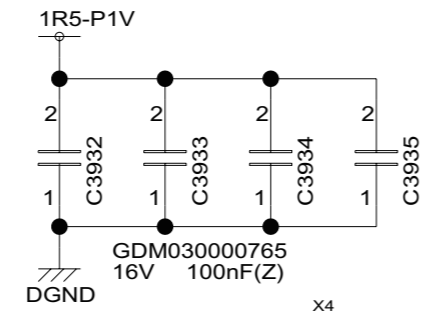
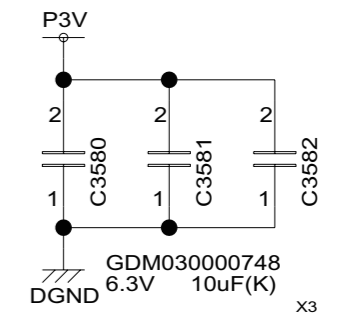
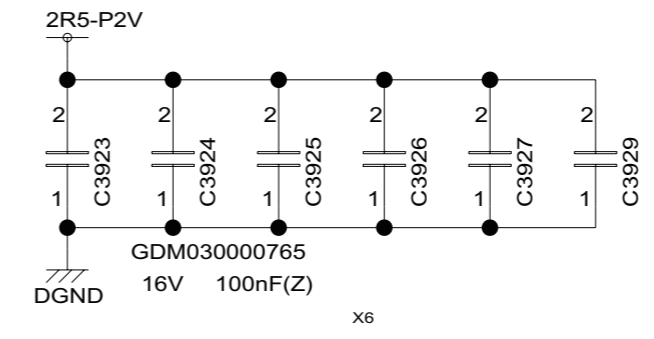
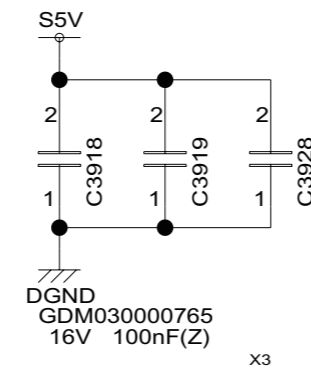
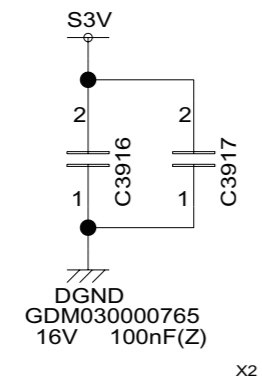
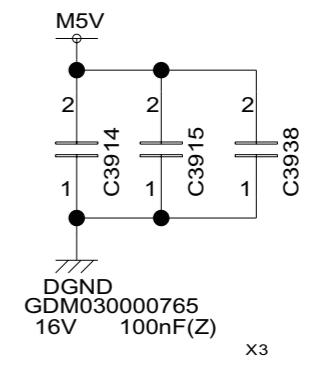
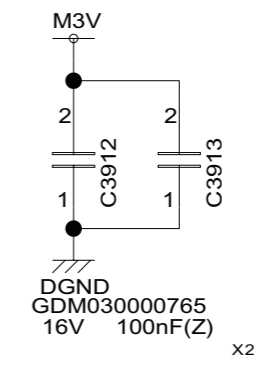
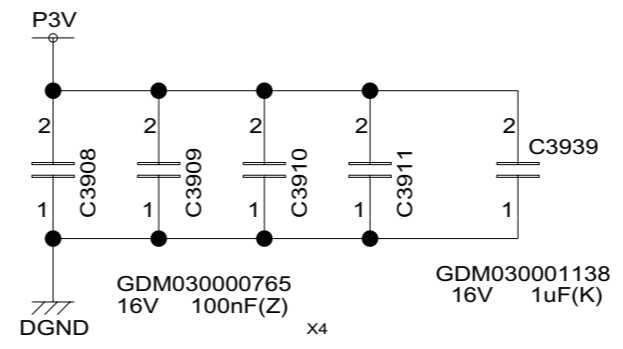
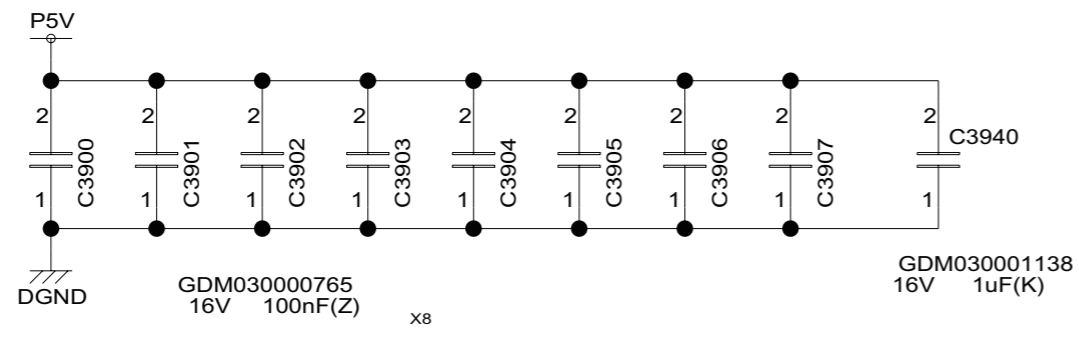
1

2

3

4

5



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